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Budker INP 2002-59

Novosibirsk
2002

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Abstract

The matter of the paper is the brief version of the Paper-Study "Pulse Power Supply System for the 10 MW TESLA Klystron" performed by BINP SB RAS under R&D contract for DESY in 1997.

The selection of the modulator for the 10 MW klystron with the 1.3 GHz operation frequency power supply designed on the 110 kV of the operation voltage, current of 130 A, pulse duration of 1.3 ms and the repetition rate of 5 Hz is proved. The operation features of the modulator and its main parts such as the high voltage power supply with constant power consumption, the high voltage pulse generator based on the mismatched pulse forming network with magnetic coupling are investigated.

The design of the low distortion high voltage feeder line on the distance up to 3 km is proposed. The pulse transformer with capacity's system of protection from breakdowns is seemed. The possibility of the pulse shape correction for its required shape providing is described. The questions of the klystron breakdown are investigated and the steps on the limiting of the energy dissipated during the breakdown are proposed.

The questions considered in the Paper-Study have had the further development both in the DESY researches connected with the high voltage power supply with constant power consumption and the high voltage cable for power distribution and in the BINP SB RAS researches of the pulse distortion during its distribution through the coaxial cable and the pulse transformer.

1 Introduction

At the present time, at many accelerating laboratories the design of electron–positron colliders at an energy of hundreds GeV and a luminosity of the order of 10^{33} is underway. Such a work is also in progress at DESY in collaboration with other accelerating laboratories. In accordance with [1], it is supposed to built at DESY an electron–positron collider TESLA–500 at an energy of 250 GeV with particle acceleration rate of up to $15 \div 25$ MeV/m and an operation frequency of 1.3 GHz for the power supply RF structures. The RF structures are to be powered from klystrons at 10 MW each, designed by the Thomson Tube Electronics. The total number of klystrons in the assembly is 604. It is supposed to set the klystrons along the accelerating structures with one klystron per 50 meters. Because the size of the tunnel is limited, the modulators for the klystrons together with a power supply are decided to be installed in kryobuildings spaced at 5 km intervals. The total number of klystrons spaced between two kryobuildings is 100.

At the same time as the TESLA–500 program is designed, a work is now underway toward the construction of the TESLA Test Facility (TTF) at an energy of 1000 MeV with a particle acceleration rate of 15 MeV/m where the number of kryomodules is 8. The power supply frequency of the RF structures is the same as for TESLA–500 and comes to 1.3 GHz. The work on TTF was started with the purpose to carry some experimental studies of the problems connected with the design of TESLA–500, and in particular of the following problems:

- obtaining the limit gradient in accelerating sections;
- developing the design and production technology of superconducting cavities;
- developing a reliable system of high frequency power supply for accelerating sections.

The elaboration of modulators for the klystron power supply in TTF is aimed at providing a series of experimental studies required for developing TESLA–500. But this project did not meet all the requirements for a future standard modulator TESLA–500. Taking into account a small required number of modulators for TTF, a question about constant power take–off from the mains is not considered. In the case of an accelerating complex with the total consumed power of several tens of MW, a steadiness of the power take–off from the mains becomes an important problem.

Each of the modulators is powered from an individual charge device. In designing TESLA–500 it is useful to estimate the advisability of the modulator power supply from an individual charge device or from a common one.

In the TTF project a modulator is installed together with a power supply near the klystron [1, 2, 3], therefore the feedline between the modulator and the step-up pulse transformer (PT), located in one tank with the klystron does not exceed one or two meters. In the design of TESLA–500, as is indicated above, the maximum distance between the modulator and klystron without regard for the tunnel depth is 2.5 km. With a regard to the real installation, the maximum distance may come to 3 km. In this connection the analysis of the effect of the feedline on the pulse parameters and calculations and design of feedline should be done. The design of the pulse transformer for the klystron power supply was done without regard for the tunnel real size where the klystron power supply system should be installed. The analysis shows that for the klystron and PT installation in the tunnel, the PT size should be reduced and its

configuration should be changed. In addition, the real value of the PT leakage inductance does not provide the pulse rise time of up to 100 μs.

The high voltage pulse on the primary PT winding in the modulator circuit [2, 3, 4] is generated by a discharge of the main capacitance C_0 to the primary winding. The pulse shape is corrected by a preliminary turn–on of the additional BOUNCER capacitance to the inductance followed by adding the capacitance voltages. The given configuration provides the required pulse quality on the klystron but requires an improved stored energy in C_0 and additional high-voltage switches and diodes for the BOUNCER. The complicated protection system against breakdowns in the klystron also demands the use of such additional elements as high–voltage switches, ignitrons, control circuits requiring a high operation reliability within a long period of time. The said above urges us to search for such designs of TESLA–500 which would lack such disadvantages. The presented paper is devoted to solving this problem.

2 The Peculiarities of a Breakdown and the Energy Released in the Klystron in the Case of a Breakdown

In accordance with the SoW, the maximum permitted energy to be dissipated in the Klystron in the case of a breakdown should be no more than 20 Joules. With the strict requirements to the maximum permitted energy to be dissipated in the Klystron in the case of a breakdown, there is a good reason to consider the case of a breakdown in the klystron in details.

Despite the fact that the vacuum insulation has been studied for tens of years and finds the use in a quantity of electrovacuum devices, to predict its behavior in the case of a breakdown is a very complicated problem. This is due to the fact that the electrical strength of the vacuum insulation depends on several factors [5]. They are:

- materials of which cathode, anode, and other parts of the device are manufactured, methods of their preparation and cleaning;
- method of preliminary evacuating and maintaining the vacuum;
- process of the device conditioning and how it reaches the operation mode;
- the energy stored in the device and in the power supply and control system elements connected with it.

Reasoning from the fact that there is always a possibility of a breakdown in the device, its electrical strength after a breakdown is specified by the energy dissipated in the device in the case of a breakdown. Let us consider a probable mechanism of a breakdown and typical time of its development.

In accordance with the data obtained by the designer on the most stressed klystron part, the minimum gap between the cathode and anode is 6 cm, and the maximum design gradients in the cathode – anode area are in the range of 67 kV/cm (on a focusing electrode) and 50 kV/cm. The klystron cathode is made of copper and the anode is made of steel. The longitudinal magnetic field strength is about 400 G in the gap.

As is known from [5], there are two phases of the vacuum insulation breakdown such as spark and arc phases. During the spark phase the voltage in the gap drops from the nominal voltage down to the arcing voltage and the vacuum gap resistance drops from infinity down to a fraction of Ohm. The typical time of a spark phase comes to 100 ns [6] for the given klystron. This value will be used in further calculations. During the spark phase the energy stored in the klystron capacity and in the elements connected to the high voltage klystron gap without restrictive resistance dissipates in the klystron. Therefore, in order to restrict this energy, there is a good reason to make a time delay for such elements or introduce restrictive resistances in the discharge circuit. We should note that there is a local energy dissipation over a short period and on a limited scale during the spark phase. Therefore there is a sufficient erosion of the electrode materials in this case.

In the case of an arc phase of a breakdown the voltage drop varies between 10 V and tens of Volts [7, 8, 9] in accordance with the arcing conditions (gap length, dimensions and materials of anode and cathode, the value of the arc current, the value of the magnetic field in the gap, etc.). The effect of the cathode material on the arc behavior is dominant because the cathode material is mainly evaporated during the arcing process. Fig. 1 shows the relation between the voltage drop on the DC arc and the cathode material in the current range up to 700 A for the gap of 0.5 cm at the electrodes diameter of 1.27 cm [7]. From Fig. 1, it is seen that the voltage drop on

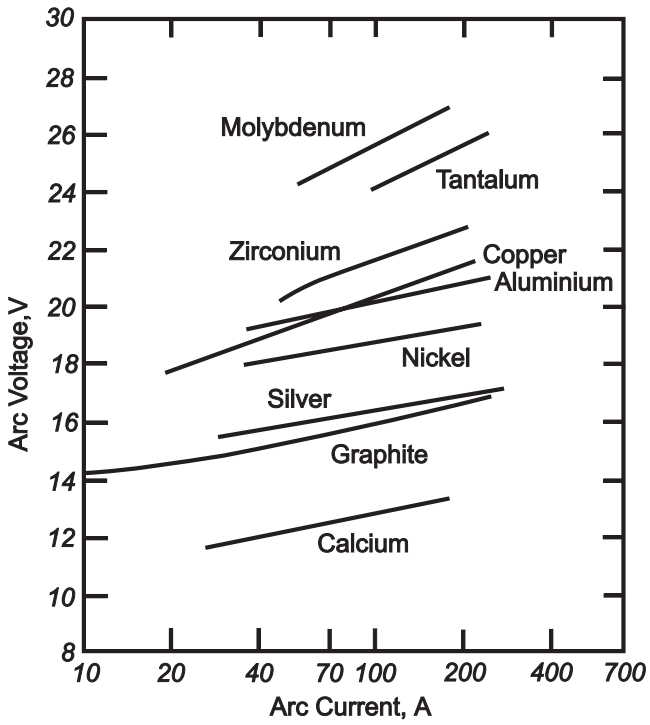

Figure 1: Volt-ampere characteristics of DC vacuum arcs [7].

the arc varies between 18 and 21 V for the copper cathode in the current range of $20 \div 200$ A. Due to the studies made in [8], with the increase of the gap between the cathode and anode the voltage drop also increases weakly. The volt – ampere characteristics of the arc discharge for the copper cathode, 5 cm in diameter, and anodes, 1.25 cm and 5 cm in diameters, with the gap of 2.5 cm (curves a and b correspondingly) and with the gap close to zero (curve c) [8] are shown in Fig. 2. From the analysis of these curves a conclusion can be made of the voltage drop not exceeding 30 V for large anodes and currents in the range of $200 \div 300$ A and the gaps in the range of $5 \div 6$ cm.

In accordance with [7], an average arcing duration for the copper electrodes and for currents of several tens Amperes makes tens of ms. Therefore, the arcing process for the given case is sufficiently stable, that is, without arc breaking with current reduction even below the point of current of extinction (for copper in the range of $1.5 \div 4$ A [5]). The arcing process is a self – maintaining process because the material vapor, first of all, the cathode material, continuously arrives at the discharge gap. The arcing process at a current of an order of tens of amperes is accounted for by several simultaneous independent arcing processes when some of them are extincted and some of them are struck. The arc spots move along the electrode surface at a rate of 10^3 cm/s and a current density of 10^7 A/cm^2. Due to this fact the energy dissipated at a local area not so big as in the case of the spark phase. During the arcing process, anode spots may appear (see Fig. 2, curve (a) for the anode 1.25 cm in diameter). Before the arc transfer to the phase with the anode spot, the arc is of a diffusive nature as applied to the anode. After such a transfer the cathode condition remains in general the same and the anode spot appears on the anode. When the anode spot is generated, the gap is filled with a vapor of

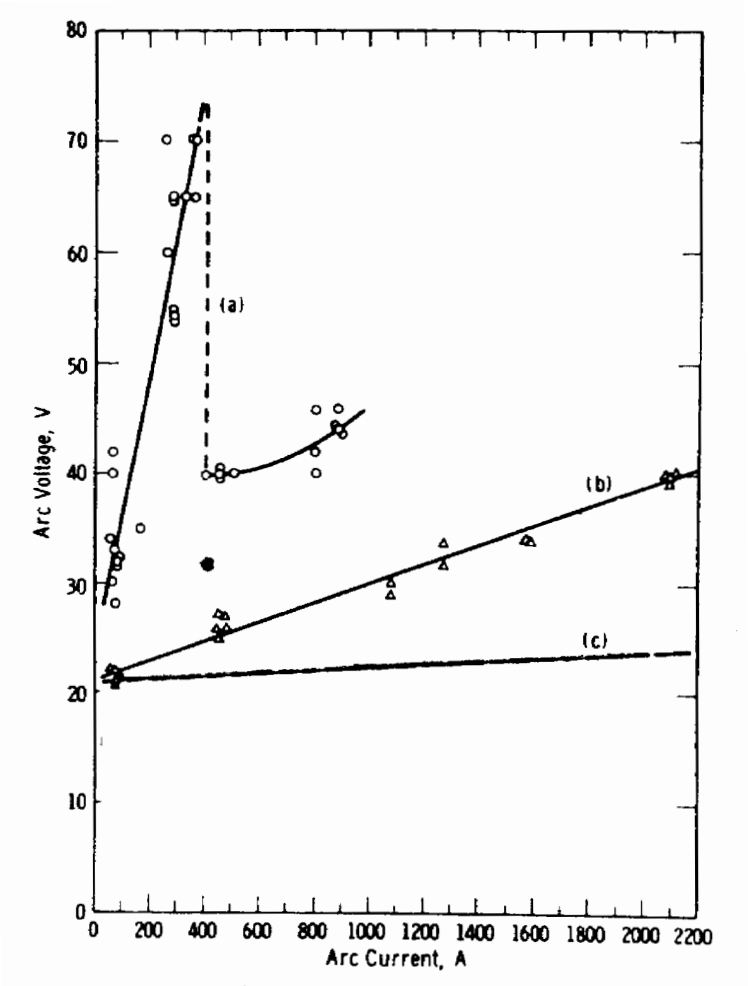

Figure 2: Volt – ampere characteristics of the arc for the cooper electrodes with different size of anode. a and b – for the gap 2.5 cm and diameters 1.25 and 5 cm, c – for the gap close to zero [8].

higher density and the arc voltage decreases. The anode spot localization causes an intensive anode disruption, therefore the rise of the process described is undesirable, because the anode spots appear at high vapor pressure of the anode materials. The arcing process continue until the current goes down below the arc confinement current. Also it is possible to interrupt the arc when the current polarity is changed. If the voltage is applied to the discharge gap in due course after the arc interruption, a following breakdown of the gap and a new cycle of arcing are possible. The effect of the longitudinal magnetic field on the voltage drop of the arc discharge has a stabilizing character according to [5, 7]. The voltage drop on the arc is stabilized and reduced, the arc transfer rate is also decreased. In view of the above reasoning the following conclusions are made:

1. A breakdown in the klystron has two phases, like spark and arc. The characteristic time for the spark phase is 100 ns.
2. In order to decrease the energy dissipated in the klystron during the spark phase, connect a minimum capacity immediately to the high-voltage klystron gap. Optional parts should be connected via restrictive resistances or via a circuit with a temporal delay.
3. The energy dissipated in the klystron during the high-current arc phase of the discharge ($200 \div 300$ A) is determined by the arc current, voltage drop on the arc (not exceeding 30 V) and arcing duration.

4. Taking into account the variety of factors specified both the klystron and its power supply which affect the energy release in the klystron in the case of a breakdown, as well as a considerable cost of the klystron and a large number of klystrons to operate at a time, there is a good reason to make a more detailed study of the klystron behavior of this type in the case of a breakdown and find the tolerable energy dissipated in the klystron in the case of a breakdown for different klystron power supply circuits.

In conclusion, it should be noted that in accordance with the recommendations of the klystron designer, it was supposed in the estimates of the energy dissipated in the klystron in the arc phase of a breakdown that the voltage drop in the arc should be no more than 200 V. In this connection when the losses in the klystron are estimated in the case of a breakdown, all the possible supply circuit solutions will be considered with regard to two maximum magnitudes of the voltage drop in the arc equal to 30 V and 200 V.

3 Design of Pulse Transformer (PT)

According to the SoW, the transformer should meet the following requirements (see Tab. 1).

Table 1: Requirements to the Pulse Transformer.

Klystron cathode voltage	110 kV
Klystron cathode current	130 A
Pulse duration (flat top)	1.3 ms
Pulse rise time	< 100 μs
Tolerance of pulse flat top	± 1 %
Repetition rate	5 Hz
Pulse transformer losses	< 1 %
Klystron filament voltage (max)	11 V
Klystron filament current (max)	60 A

The pulse transformer can be mounted horizontally. Its overall cross dimensions should not exceed 1.2 m in width and 1.4 m in height because of a limited space in the tunnel. The transformer should have a minimum leakage inductance.

The general design of PT is specified by a magnetic system (MS) type. A pivotal twisted MS of a split type is used to power klystrons in high-powered PTs. Fig. 3 shows one of those transformers manufactured by Stangenes Industries, Inc., USA. Primary and secondary windings divided into two parts are installed on the MS rods. Taken alone, the MS is made up of some equivalent twisted cores of a split type. For high pulse duration such a constituent core is required and it has no alternatives. Therefore, we suppose to consider a similar MS. Most popular electrical cold-rolled steel 3425 is used for the magnetic system production. Such steel has a large saturation induction and being annealed it is characterized by a small coercive force $H_c = 32\ \frac{\text{A}}{\text{m}}$. Characteristics of the steel are listed in [10].

Table 2 presents the values of the average relative magnetic permeability μ_Δ taken in accordance with the curves of the 3425 steel magnetization for those field induction values which are in the region of our concern. Because the pulse energy is large and equal to 20 kJ, the MS should be of a large size. Therefore, we take the induction increment equal to $\Delta B = 2.8$ T, which is close to the maximum value of steel 3425. In order to obtain the accepted induction increment, the demagnetizing field brought from the external source is designed. For the length of the MS line of force equal to $l = 2.135$ m the required back ampere turns are as follows

$$iw \geq H_C l \geq 68.5 \text{ A}.$$

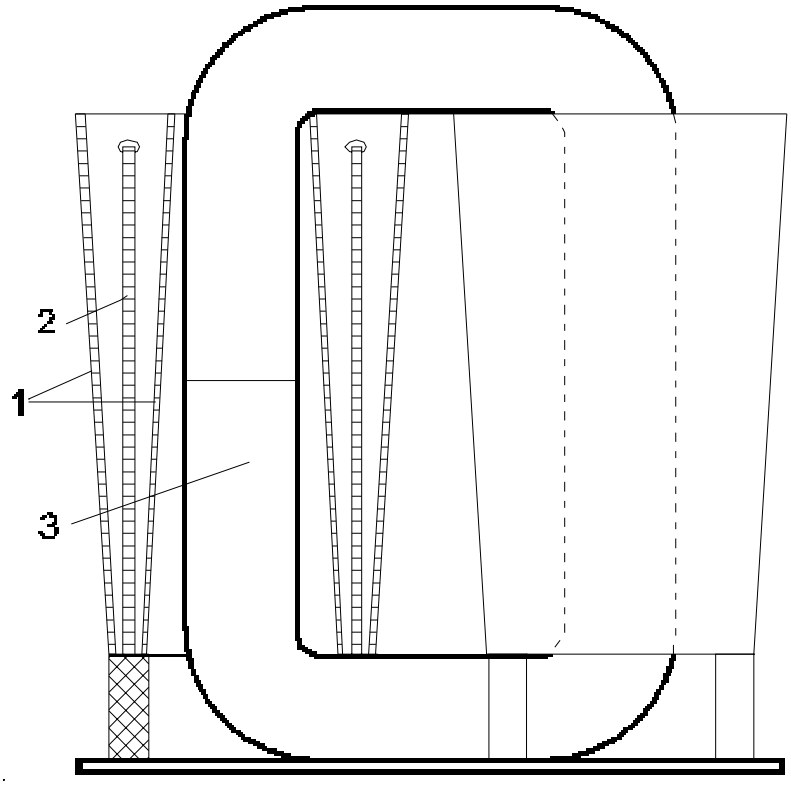

Figure 3: Pulse transformer manufactured by Stangenes Industries, Inc., USA. 1 – primary winding; 2 – secondary winding; 3 – core.

Table 2:

B, T	1.2	1.4	1.5	1.6	1.7
H, $\frac{A}{m}$	50	100	158	300	600
$\mu_\Delta \cdot 10^3$	21.0	12.5	8.1	4.4	2.15

As a rule, the secondary winding in such a PT is designed on a common framework of pyramidal shape. The high-potential winding edge is designed with rounded edging of the required radius of curvature.

The proposed version provides two secondary windings on each MS rod where high voltage is tapped in the middle. In addition, two primary windings of pyramidal shape where the high voltage is tapped on the ends are fitted. The electrical circuit and the diagram of the transformer winding positioning are shown in Fig. 4 and Fig. 5.

Owing to the fact that the windings are identical and connected in parallel, the voltage increases from 0 up to U_2 gradually throughout the height of the bottom secondary winding and gradually decreases from U_2 down to 0 throughout the height of the upper secondary winding. As a result, there is no sudden voltage change at a single point between the windings and the electric field strength in the inter-winding space is constant throughout the winding height, so the edge effect is fully ruled out. This allows to choose the minimum value of the main insulation, that is, to make the best use of the insulation properties of surrounding (transformer oil or SF_6).

In order to make the best use of the steel magnetic properties of the core, the PT has a demagnetizing winding connected with an external current source.

The primary windings of pyramidal shape decrease significantly the PT leakage inductance as the inter-winding capacity slightly increases.

Each of the secondary windings has 15 sections (see Fig. 12). Each section has 48 turns of

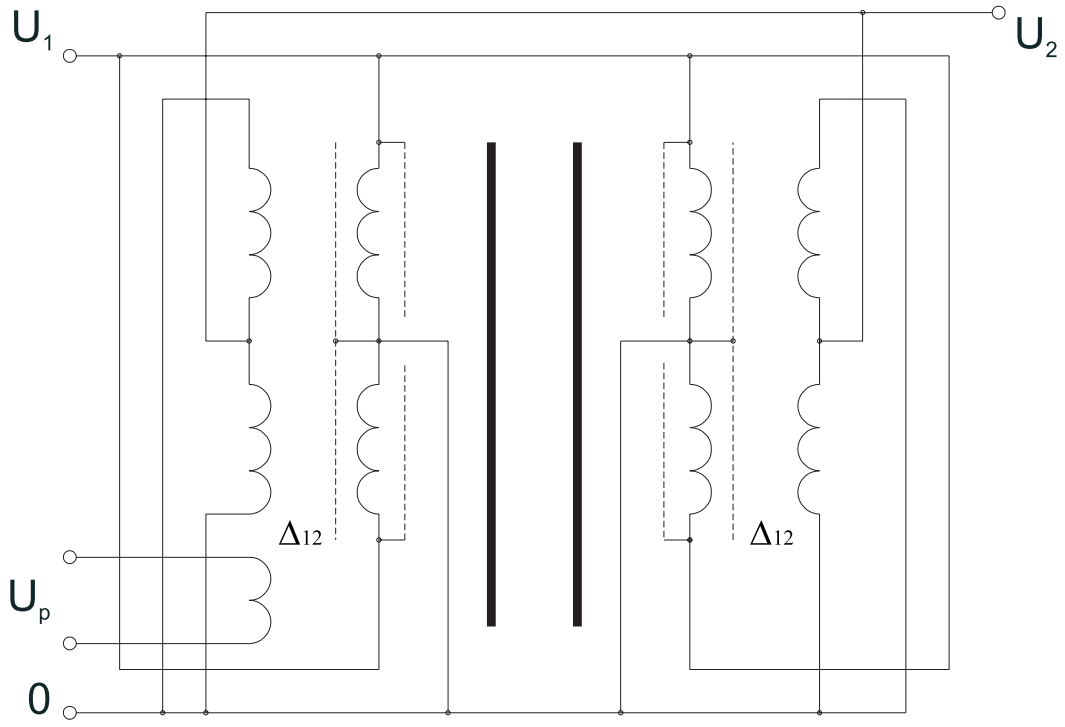

Figure 4: Electrical circuit of transformer with four-sectional secondary winding with output in the middle point.

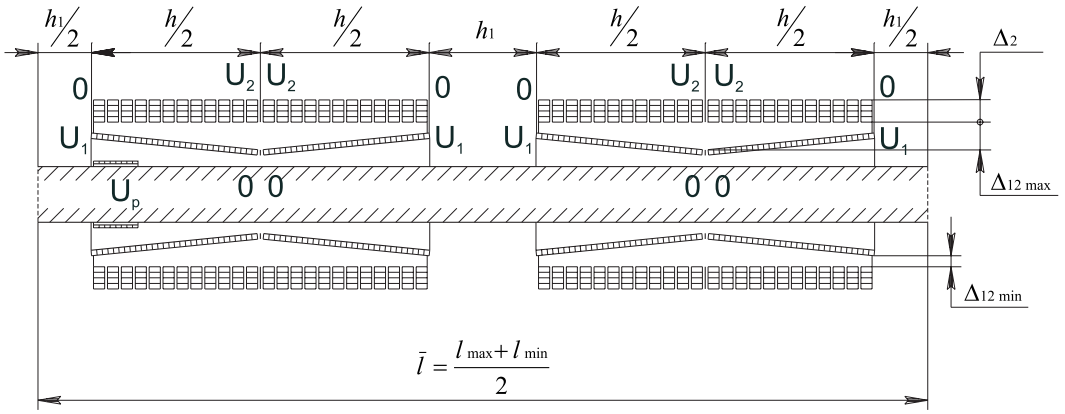

Figure 5: Diagram of positioning and connecting the windings in the transformer.

a rectangular conductor 1.32×4.0 mm^2 in cross section. Each section is impregnated with an epoxy compound and has a shield with rounded edges.

In order to reduce the longitudinal voltage gradient at breakdowns in the system, each section is equipped with ceramic capacitors which increase the longitudinal capacity of the secondary winding.

The characteristic property of the designed PT is the necessity to join the cathode high-voltage klystron electrical termination designed to be operated in the transformer oil with a high-voltage electrical termination of the PT. Taking into account this property, Fig. 6 presents one of probable versions of PT and klystron general layout.

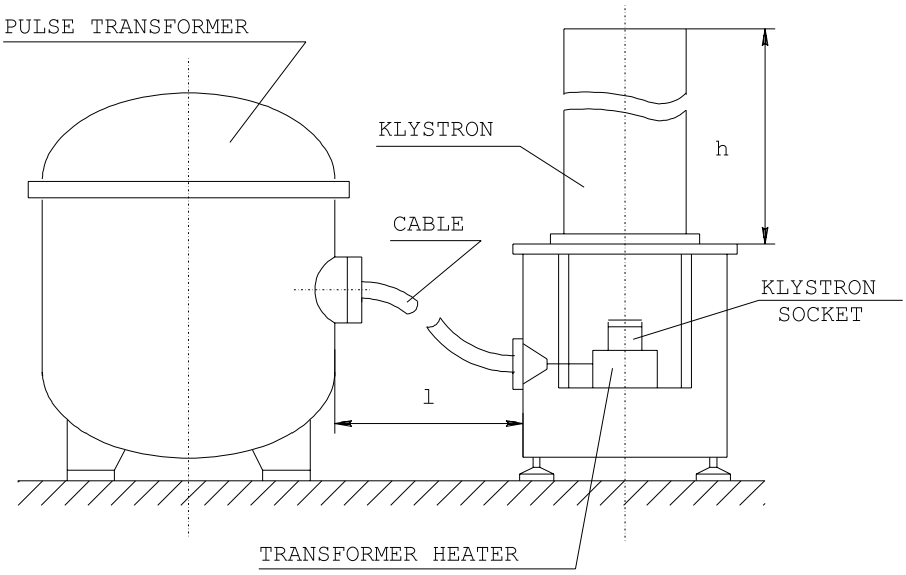

Figure 6: Version of PT and klystron layout.

3.1 Deciding on Insulating Surroundings and Working Insulating Gradients

The PT windings should meet the basic requirements:

- sufficient electric strength;
- minimum leakage inductance, dynamic capacitance and resistance;
- sufficient mechanical strength.

The requirements on the electric strength and minimum leakage inductance are discrepant. That is, it is necessary to increase the insulation width for improving the electric strength, whereas the reduction of leakage inductance requires to decrease the insulation width. The capacitance reduction in its turn is in conflict with the requirement of minimum leakage inductance for the same reasons.

In the case under consideration the reduction of the leakage inductance is more important than that of the capacitance. Therefore the inter-winding dimensions are minimized as required by the winding electric strength. In this connection the insulation materials with a low dielectric permeability and a high electric strength are used for the PT under consideration.

3.2 Main Insulation

The transformer oil (relative dielectric permeability is $\varepsilon_r = 2.2$) and SF_6 ($\varepsilon_r = 1.0$) which meet the listed requirements are best suited insulation materials for the main insulation. Comparative characteristics of different insulation media are given in Fig. 7. According to proposals of [10], the

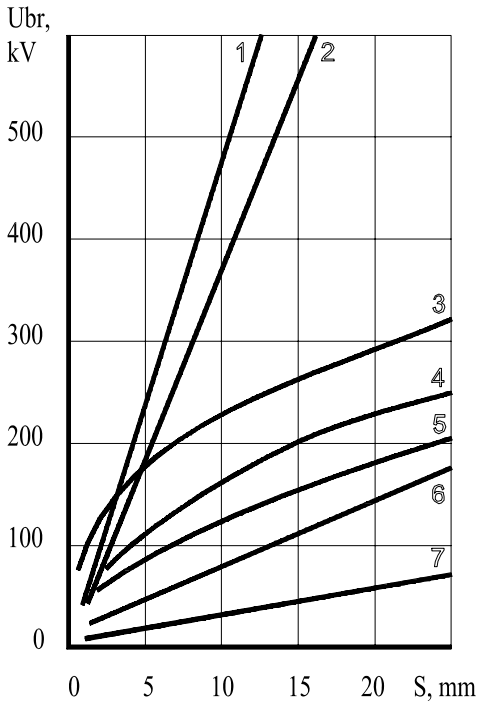

Figure 7: Relationship between breakdown voltage and distance between electrodes. 1 – air at a pressure of $2.8 \cdot 10^6$ Pa; 2 – SF_6 at a pressure of $7 \cdot 10^5$ Pa; 3 – high vacuum; 4 – transformer oil; 5 – electro-ceramics; 6 – SF_6 at atmosphere pressure; 7 – air at atmosphere pressure.

electric field strength of approximately 10.0 MV/m is allowable for a all-oil insulation. For the SF_6 insulation the electric strength depends on the gas pressure, and when the excessive pressure is equal to $0.7 \cdot 10^5$ Pa it comes to 13.0 MV/m. The adopted width of the main insulation is equal to 38.5 mm and the average electric field strength comes to 2.85 MV/m. Fig. 8 shows the electric field in the high-voltage edge area of the windings. Fig. 9 gives the electric field strength on the shield at 110 kV. The maximum strength on the shield over two times exceeds the average strength and comes to 5.9 MV/m. Consequently, the electric field strength is chosen with the required reserve of strength.

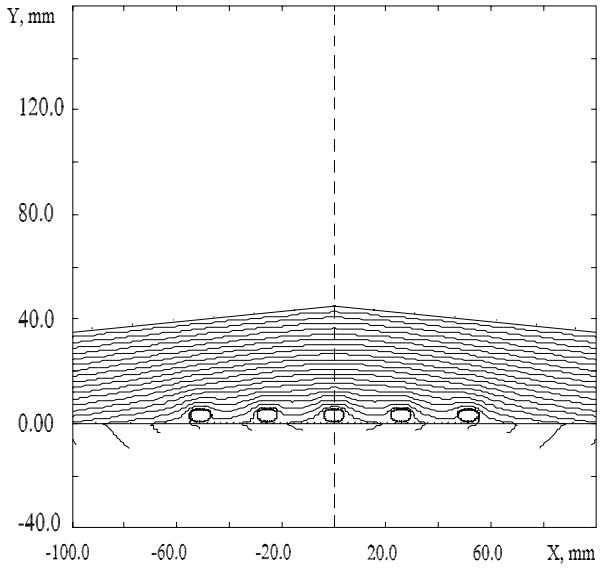

Figure 8: Electric field in the high-voltage edge area of the secondary winding.

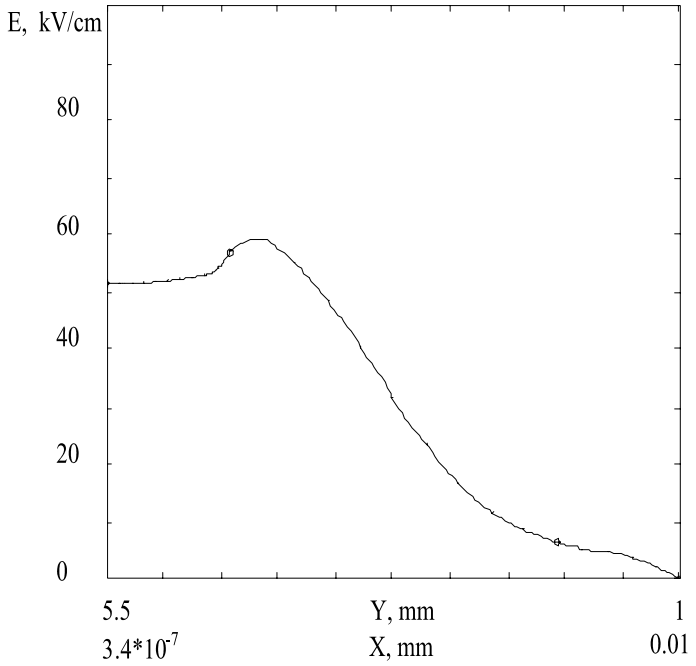

Figure 9: Electric field strength on the shield at 110 kV.

3.3 Longitudinal Insulation

The secondary winding has 720 turns and falls into 15 separate sections. It is wound with a PSD conductor (that is the Russian type PSD conductor with the alkaline-less fiberglass insulation of two layers glued and impregnated with a heat-resistant varnish/lacquer), 1.32×4.0 mm^2 in cross section. The cross section with the insulation is equal to 1.74×4.32 mm^2.

Each section of the winding is wound as a spiral with four turns in each layer. There is an even number of layers in the spiral winding and the directions of adjacent layers are opposite, two layers being wound with once conductor without interruption. Such a type of winding allows to connect the upper and bottom layers on the outside, that is, the end of one layer is connected with the end of another or the beginning is connected with the beginning. The transition between the layers is located in the area of unipotential turns to form a more reliable design. A 0.22 mm thick paper is applied as a layer-to-layer insulation. The section is impregnated with an epoxy compound.

The longitudinal electric field strength comes to 1.7 MV/m and it is in correspondence with the data given in [11].

The primary winding ($w_1 = 60$ turns) is wound as one layer with the PSD conductor with a cross section of 4.0×5.6 mm^2 (4.47×5.92 mm^2 with insulation) with the electric strength of 600 V. The nominal turn-to-turn voltage is 153 V/turn.

3.4 Winding Protection against Over voltage

During the klystron operation there may occur abnormal regimes of open – circuit and of short – circuit. With the open – circuit the generator voltage will be increased. In this connection the PT should have some reserve of electric strength. And make sure that the voltage steps are applied evenly to the winding turns.

Let us take a look at the secondary winding operation when the step steep pulse lasting for a fraction of a microsecond excites it (see Fig. 10). When such a wave gets to the potential end of the winding, the voltage increases rapidly. The process rate is so high that at first a current does not come through the winding turns because of their large inductance and travels over the capacitive circuit of the winding. Taking the height of the secondary winding to be unity, the

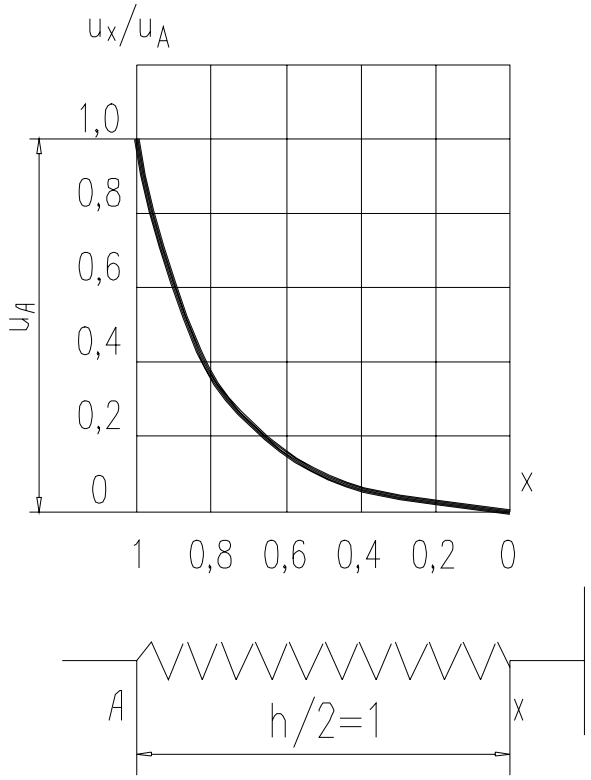

Figure 10: Voltage distribution throughout the sections of the secondary winding for $\alpha = 5$.

voltage distribution for the uniform capacitive circuit takes the form (see [12]):

$$u_x = u_A \frac{\sinh \alpha x}{\sinh \alpha}.$$

In this formula such a parameter as

$$\alpha = \sqrt{\frac{C_q}{C_d}} = n\sqrt{\frac{C'_q}{C_d}}$$

completely determines the nature of the voltage distribution. Here n is the number of winding sections, C_d is the total longitudinal winding capacitance equal to $\frac{1}{n}C'_d$, C_q is the total transverse winding capacitance equal to nC'_q, C'_d is the referred section capacitance, C'_q is the section capacitance towards the grounded shield of the primary winding.

The referred section capacitance is calculated with a consideration for the type of layers application when the voltage at the layer-to-layer insulation varies between 0 and a two-fold magnitude of the one layer voltage. Therefore

$$C'_d = \frac{4}{3}\frac{\varepsilon_0 \varepsilon_r S}{\sum \Delta} = 252 \text{ pF},$$

where $S = 4.74 \cdot 10^{-2}$ m^2 is the area of the layer-to-layer insulation, $\sum \Delta = 8.8 \cdot 10^{-3}$ m is a summarized thickness of the layer-to-layer insulation, $\varepsilon_r = 4$ is a relative dielectric constant of the insulation. Then

$$C_d = \frac{1}{n}C'_d = 16.8 \text{ pF}.$$

The transverse winding capacitance calculated from the averaging gap $\overline{\Delta}_{12}$ between the windings comes to:

$$a) \qquad C_q^0 = \frac{\varepsilon_0 \varepsilon_r S}{\overline{\Delta}_{12}} = 662 \text{ pF},$$

when the main insulation is the transformer oil ($\varepsilon_r = 2.2$), and

$$b) \qquad C_q^0 = \frac{\varepsilon_0 S}{\overline{\Delta}_{12}} = 302 \text{ pF},$$

when the main insulation is SF_6 ($\varepsilon_r = 1$).

The transverse winding capacitance towards the PT housing C_q^k is estimated approximately and comes to:

a) for the transformer oil $C_q^k = 110$ pF;

b) for SF_6 $C_q^k = 50$ pF.

Then the total transverse capacitance is $C_q = C_q^0 + C_q^k = 772$ pF (for the transformer oil) and 352 pF (for SF_6).

The maximum voltage gradient will be in the high-voltage coil end and equal to

$$\left(\frac{du}{dx}\right)_{x=1} = \frac{u_A}{1}\alpha \coth \alpha.$$

With $\alpha > 3$,

$$\left(\frac{du}{dx}\right)_{x=1} \approx \alpha \frac{u_A}{1}.$$

In the case being considered there is a parameter α calculated from the averaging gap which is equal to

$$a) \ \alpha = \sqrt{\frac{C_q}{C_d}} = 6.78,$$

when the main insulation is the transformer oil and

$$b) \ \alpha = 4.58,$$

when the main insulation is SF_6.

Thus the high-voltage coil end is loaded 6.78 – or 4.58 – fold compared to the mean value. In order to eliminated this effect, the ceramic low-inductive capacitors are installed increasing the longitudinal winding capacitance. In this case to reduce the voltage gradient by half, the longitudinal winding capacitance should be increased four times. For this purpose the capacitance for the oil $C_p \approx 1000$ pF and $C_p \approx 460$ pF for SF_6 should be set up. Thus, by an insufficient increase in the PT capacitance, an over voltage can be significantly reduced. The referred circuit capacitance C_2' made up of C_q and C_d is equal according to [12] to the following:

$$C_2' \approx \sqrt{C_q C_d} = \alpha C_d = 114 \text{ pF}$$

for the transformer oil and 77 pF for SF_6.

The referred capacitance of the whole PT with four secondary windings connected in parallel is equal to $C_2 = 4C_2' = 456$ pF for the oil and $C_2 = 308$ pF for SF_6 without C_p.

The primary winding will be protected against the over voltage in a different way, which is illustrated in Fig. 11.

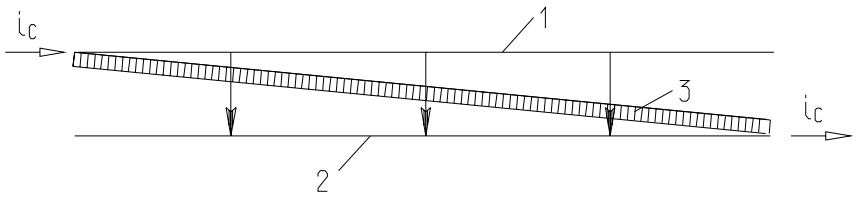

Figure 11: Method of protection of the primary winding. 1, 2 – shields; 3 – winding.

The principle of this method of protection is that the winding turns are inserted between the electric field produced by winding shields. In this case the winding turns are located in such a manner that each turn is located on its equipotential line. In this case the capacitance current transfuse the turns, but does not run along the turns, thus, it does not distort the even distribution of the voltage over the turns.

3.5 PT Design

Eight split cores 2 are placed with the gap 5 mm apart on the base 1 (see Fig. 12). The cores are wrapped with a 0.15×80 mm^2 tape, impregnated with an epoxy compound and cut into two equal parts. The bottom parts of the core are screwed to the base. The upper parts are separable and bound to the bottom parts with tape clips 3. The support frame 4 where the

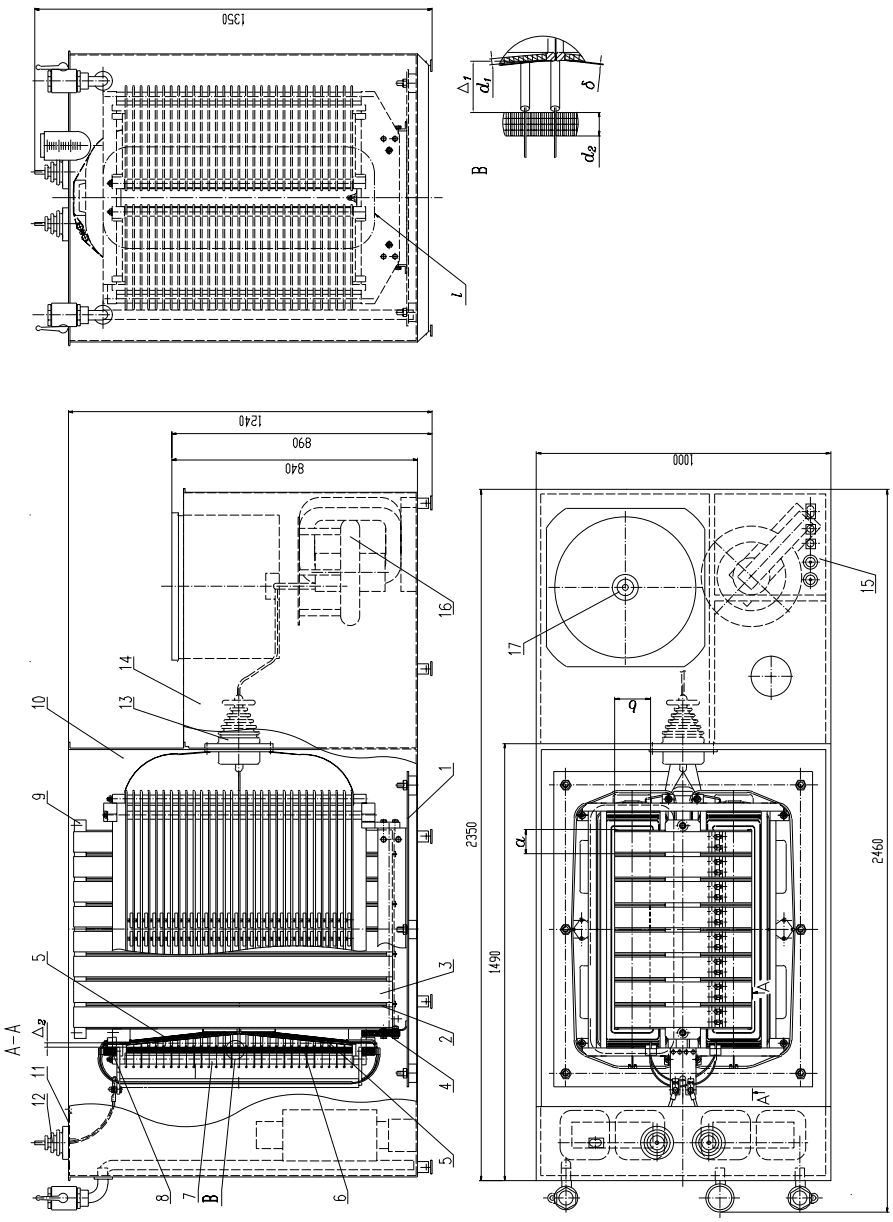

Figure 12: Pulse transformer. 1 – base, 2 – split cores, 3 – tape clips, 4 – support frame, 5 – primary winding, 6 – secondary winding sections, 7 – insulating ties, 8 – upper forcing frame, 9 – channel section, 10 – transformer tank, 11 – transformer connectors, 12 – input, 13 – output, 14 – klystron tank, 15 – klystron connectors, 16 – heater transformer, 17 – klystron socket.

primary windings 5 are mounted is installed on the base. The secondary winding sections 6 connected in electric series are installed on the frame in turn. Four insulating ties 7 screwed into the support frame align the sections during their installation. Each limb of the core contains 15 bottom and 15 upper sections distinguished by a direction of applying.

The upper forcing frame 8 is installed on two upper sections. By means of the frame 8 a set of 60 sections is fixed by the ties 7 as a whole. When all the windings have been installed, tied and commutated, the separable parts of the core are installed in turn. The channel section 9 is installed on the top of the cores, then all eight cores are tied with the tape clips. Freight ring-bolts are screwed into the channel and the transformer assembly is installed into the transformer tank 10, covered with an elliptical top 11. The pulse transformer has an input 12 and an output 13 leads.

Secondary Winding Design

The section is designed as a rectangular frame with dimensions 357×944 mm^2 (see Fig. 13). The height is 25.6 mm. The winding consists of 48 turns and is wound with a PCD conductor with dimensions 1.32×4.0 mm^2 (copper). Each section has six subsections with 8 turns in each. The subsections are connected along the small outer side of the rectangular frame. The assembled section is impregnated with an epoxy compound in a compression mould to the required dimensions and shape. A foiled glass-textolite plate with the edge piped with stainless steel, 6×1 in dia, is glued to the frame end. Low-inductive ceramic capacitors are installed on a free plate area.

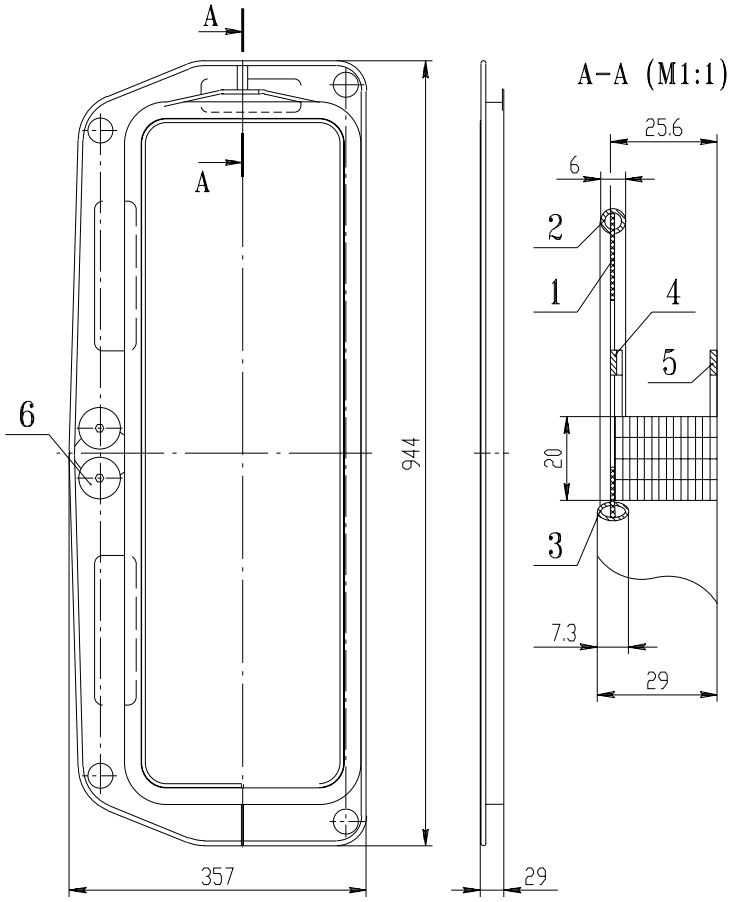

Figure 13: Secondary winding section. 1 – base; 2 – exterior shield; 3 – interior shield; 4 – winding begin; 5 – winding end; 6 – capacitor.

3.6 Basic Transformer Parameters

Voltage under load, kV	110
Load current, A	130
Pulse duration, s	$1.3 \cdot 10^{-3}$
Pulse rise time, s	10^{-4}
Transformation ratio	12
Number of secondary winding turns	720
Energy to load, kJ	20
Energy heat losses, %	1
Repetition frequency, Hz	5
Referred capacitance (for SF_6), pF	308
Referred capacitance (for oil), pF	456
Magnetization inductance reduced to primary circuit, H	1.13
Leakage inductance reduced to primary circuit, H	1.9×10^{-4}
Core section, m^2	7.1×10^{-2}
Length of the core force line, m	2.265
Core weight, kg	1260
Overall dimensions:	
height, m	1.35
width, m	1.0
length, m	2.35

Resume

1. The suggested transformer design with the windings connected in parallel allows to reduce the electric field strength on the high voltage end of the secondary winding as well as to minimize the leakage inductance.

2. The secondary winding design allows to reduce over voltage between winding turns and effectively protects the transformer at full voltage breakdowns.

4 Pulse Former (PF) of the rectangular pulse

The initial data for analyzing the PF circuits are SoW, the parameters of a klystron, and the pulse transformer (see Section 3). The pulses with a voltage $U_{kl} = 110$ kV, a current $I_{kl} = 130$ A and a pulse duration ~ 1.4 ms can be generated both with the use of PT and without it. In order to generate pulses without PT, it is necessary to use a controlled high-voltage switch or a klystron with an anode or a grid modulation. Nowadays, there are no industry-made switches of the considered power and pulse duration. Disadvantages of the generator with the anode modulation are given in [17]. The pulses generated with the use of PT can be based on voltage [16, 17] or current sources [16, 17, 18]. Modulators based on a current source (SMES) will not be considered in the present paper.

An artificial pulse forming network (PFN) [16, 17] or a partially discharging capacitor bank with a correcting circuit BOUNCER (B-modulator) [3, 4] can be used as PF.

4.1 B-Modulator Circuit

The B-modulator circuit was suggested by Fermilab and described in details in [3, 4, 17]. Using this circuit as the base, Fermilab designs modulator [4] of the parameters listed in Table 3 (New Modulator). The circuit presented in Fig. 14 corresponds to the latest model of the modulator. We shall take a quick look at this circuit operation. The main capacitor bank, C_0, is charged to a value which is by approximately 10% higher than required output voltage, while the BOUNCER, L_1&$C1$, is charged to 15% of the required output voltage. To produce an output

Table 3: The original and new modulator parameters.

	Original Modulator	New Modulator
Pulse Width (+/- 0.5%)	2.0 ms	1.4 ms
Output Voltage	130 kV	110 kV
Output Current	95 A	130 A
Repetition Rate	10 pps	10 pps

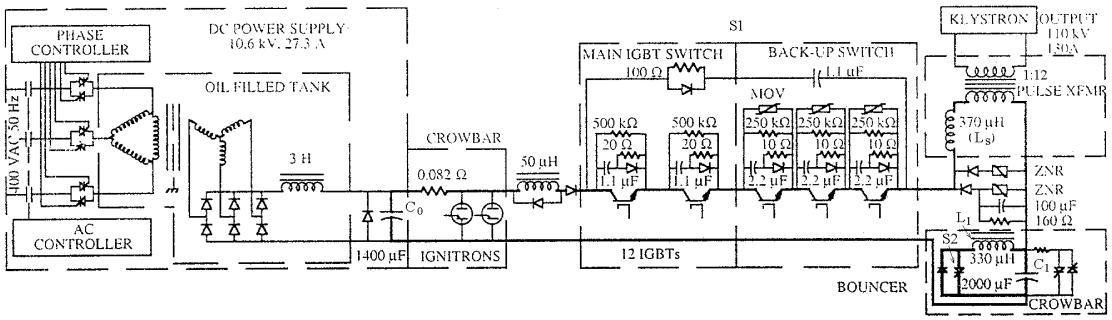

Figure 14: Overall schematic of modulator.

pulse, the bouncer voltage is subtracted from the main capacitor bank voltage by following. The BOUNCER resonant circuit switch, S_2, is closed, and the capacitor C_1 starts to ring with the inductance L_1. At the appropriate time the switch S_1 connects the main capacitor bank C_0 to the pulse transformer. After the output pulse length, the switch S_1 disconnects the capacitor bank C_0 from PT. The bouncer circuit continues then to ring through the full cycle. Fig. 15 shows the waveforms on the bouncer circuit and the main capacitor bank and Fig. 16 shows the total output voltage in full size and expanded versions.

Unlike the first version of the modulator [3], the new one [4] has a switch based not on the GTO thyristors but IGBT transistors. As a basic switch, the IGBT is an easier device to use. Its insulated gate requires a drive circuit to drive only a capacitive load. The gate drive peak power and average power are each of approximately five times lower for the IGBT than for the GTO. The IGBT has approximately one tenth of the turn-on and turn-off times of the GTO. The choice of the devices was based on the requirements to the pulse transformer primary circuit. The switch assembly must conduct a 1.6 kA pulse for 1.7 ms and block about 13 kV in the off state.

The operation of the described modulators over a long period of time has shown its high reliability both in the operation regime and at a load breakdown. It seems worth while to highlight the main features of this circuit. The main capacitor bank operates in this circuit with a partial discharge thus providing for the use of filter capacitors with a higher specific power intensity. The IGBT switch controls the pulse duration and cutoff the capacitor bank from the klystron power supply circuit at the klystron breakdown. But an auxiliary BOUNCER circuit with a pre-closed switch which requires some initial voltage on the circuit capacitor adds some complexity to the circuit. Also it can be noted that the main capacitor bank has a large stored energy that also complicates the protection of the klystron and switch in case of the klystron (or switch) breakdown.

4.2 Circuits based on the PFN. Matched PFN

As was mentioned above, along the circuit with a partial discharge of the capacitance with a BOUNCER for the purpose of forming rectangular pulses one can use a PFN (see Fig. 17), which operate both in matched ($\rho = R_{load}$) and mismatched ($\rho \neq R_{load}$) mode (ρ is the wave impedance, R_{load} is the load resistance).

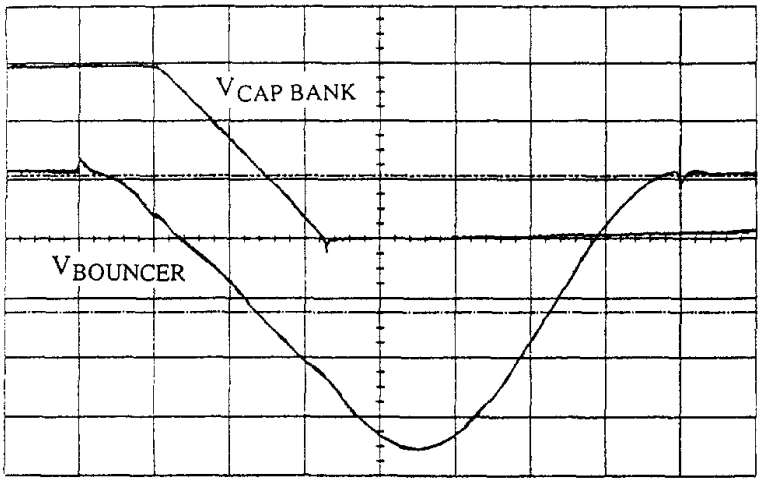

Figure 15: Main capacitor bank voltage (top) and bouncer voltage (500 V/div, 1 ms/div, main capacitor bank zero suppressed).

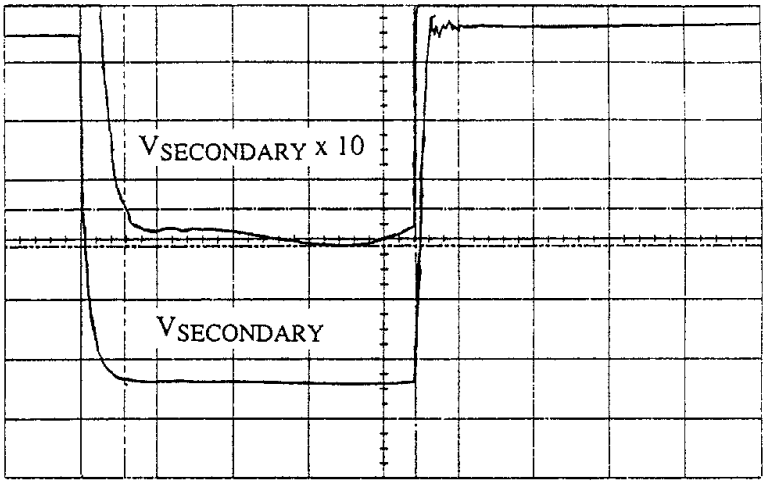

Figure 16: Expanded secondary voltage (top) and secondary voltage (2 kV/div, 20 kV/div, 0.5 ms/div, expanded zero suppressed).

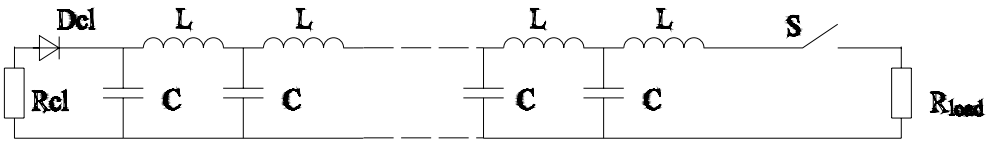

Figure 17: The base circuit of a PFN.

It is convenient to characterize the mismatch coefficient between the PFN and the load with the coefficient α:

$$\alpha = \rho / R_{load}.$$

The value of $\alpha = 1$ corresponds to the matched mode. The PFN charge voltage $U_{pfn}(0)$ is defined by the expression:

$$U_{pfn}(0) = U_{load} \frac{R_{load} + \rho}{R_{load}} = U_{load}(1 + \alpha), \tag{1}$$

where U_{load} is the voltage on the load. The cell inductance L and capacitance C of the ladder PFN with the number of cells n can be defined by the following expressions ([16, 19]):

$$L = \frac{t_p \alpha R_{load}}{2n}, \quad C = \frac{t_p}{2n\alpha R_{load}}. \tag{2}$$

Here t_p is the pulse duration with taking into account the rise time t_{rt} and fall time t_f ($t_p = t_{rt} + t_{top} + t_f$).

Matched PFN

The following properties of the matched PFN in operation should be mentioned:

- the pulse amplitude, formed by the matched PFN, makes one half of the charge voltage;
- in the operation mode the capacitor banks of the PFN are completely discharged;
- the pulse fall time is formed by the network itself, therefore it is not necessary to use a controlled IGBT switches, as in B-modulator or mismatched PFN;
- estimates show that the total cell inductance for the matched PFN ($\rho = 5.88$ Ohm, $t_p = 1.4$ ms) makes $L_\Sigma = 4.4$ mH.

The following features can be added to the advantages of this circuit:

- The opportunity of using not so expensive thyristor switches as compared to expensive IGBT switch in B-modulator or PF based on mismatched PFN.
- The problem of restricting of energy dissipated in the klystron at a breakdown can be easily solved if the voltage drop on an arc is taken as $U_{arc} \approx 30$ V (see Section 2). Really, the clipper circuit assembled at the end of the network (resistor R_{cl} and diode D_{cl} in Fig. 17) absorbs almost all the energy stored in the PFN capacitors within a period of time $t_{arc} \leq t_p$. In this case the energy in the arc does not exceed $W_{arc} = I_{arc} U_{arc} t_{arc}$ due to the arc current limitation with a PFN impedance ($I_{arc} = U_{PFN}(0)/\rho = 2I_{kl}$). At $I_{arc} = 260$ A, $U_{arc} = 30$ V, and $t_{arc} = 1.4$ ms, the energy released in the arc comes to 10.9 J.

  The losses in the spark do not exceed $W_{spark} \leq W_{Cpt} + W_{Ckl}$ if the klystron is fed through the low voltage feedline. Here W_{Cpt} and W_{Ckl} is the energy stored in the PT and klystron capacitances, respectively. With the klystron voltage being $U_{kl} = 110$ kV, the capacitance of the PT being $C_{PT} = 456$ pF and at the capacitance of the klystron being $C_{kl} = 50$ pF, the energy stored there comes to 2.75 J and 0.3 J, respectively. Thus, the total losses in the klystron are less than 14 J in the case of a breakdown, that is, they do not exceed the permissible value of 20 J (see SoW).

The following features can be mentioned as the disadvantages of this circuit compared with mismatched PFN or B-modulator:

- the large PFN cell inductance which causes losses in the coil copper and increases the overall PFN dimensions. This complicates its implementation;

- more intensive operating mode of the cell capacitors because the PFN discharges completely;
- the larger pulse fall time because in the case of matched PFN it is generated by all PFN cells. This causes a decrease in PF efficiency.
- a two-fold (compared to the load voltage) charging voltage on the PFN complicated the design of high voltage components of the modulator.

As it was mentioned above in order to estimate the energy dissipated at the klystron breakdown the klystron designers (Thomson Tubes Electronics) suggest to use the magnitude of the voltage drop in the arc equal approximately to 200 V. In this case the energy released in the arc during one pulse essentially exceeds a permissible (according to SoW) value. Therefore, it is necessary to use an additional protection system against the klystron breakdowns. This makes the design of the PF based on matched PFN more complicated and not reasonable.

4.3 Circuits based on mismatched PFN

A mismatched PFN has some advantages over a matched PFN circuit. In such a PFN one can use less expensive capacitors as cell capacitance with a large specific storage energy. The total inductance of the mismatched PFN can be sufficiently smaller than the inductance of the matched PFN; its decreases the losses, dimensions and cost of the PFN. In this case the high voltage design of the modulator elements is also simplified due to a lower charging voltage (in comparison with a matched PFN).

One of the important characteristics of the mismatched PFN is its coefficient α. It is presented in [21] that with the decrease of α of the ladder PFN the pulse rise time and oscillations on the pulse flat top decreases and tend to 0 at $\alpha \to 0$. However, when the PFN operates with a load connected through the PT the pulse rise time is determined mainly by the PT leakage inductance L_s. The dependence of the pulse rise time on α for the mismatched PFN will be found below.

4.3.1 Ladder PFN

The pulse shape formed by ladder PFN was analyzed based on the circuit given in Fig. 18. Here the klystron is presented as a linear resistance R_{load} and diode D connected in series. The value R_{load} (the referred klystron resistance) is equal to $R_{load} = \frac{U_{kl}}{I_{kl}} \frac{1}{k_{pt}^2}$, here U_{kl} and I_{kl} are the klystron voltage and current, k_{pt} is the PT ratio. Preliminary calculations are made

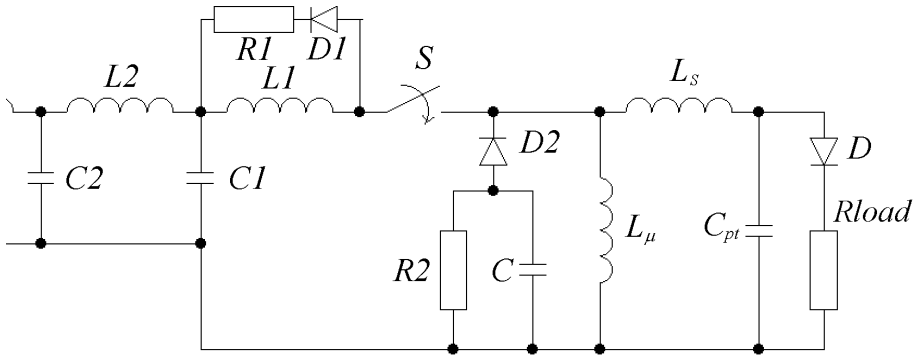

Figure 18: The circuit for simulation the pulse shape formed by ladder PFN.

without taking into account the nonlinear volt – ampere characteristic (VAC) of the klystron. The actual VAC of the klystron will be taken into account in final calculations. At $t = 0$ the

switch S connects the PFN to the load and disconnects at the end of the pulse. We impose the condition of $L_1 \geq 50$ μH on the inductance of the first PFN cell L_1, because it is necessary to limit the current through the switch at a breakdown in the primary circuit of PT. The value of the inductance L_1 is chosen the same as in the B-modulator [4]. The circuit of a diode D_2, resistor R_2, and capacitance C proposed in [3, 4] requires to dissipate the energy stored in the PT within a pulse duration. The circuit $R_1 D_1$ absorbs the energy stored in L_1 towards the end of the pulse. Since the shape of the pulse rise time depends only on the parameters of the first cell (L_1&C_1) then in order to obtain the minimum pulse rise time, when the flat top irregularity is $\leq 2\%$, the inductance L_1 and capacitance C_1 have been corrected. Fig. 19 shows the dependence $t_{rt}(\alpha)$ at number of cells $n = 10, 15, 20, 25$. From this figure it follows that in the range of small $\alpha \leq 0.2$ the pulse rise time scarcely depends on the number of cells n (if $n > 10$). From the obtained data it follows that t_{rt} can be reduced with increasing α only provided that n is also increased.

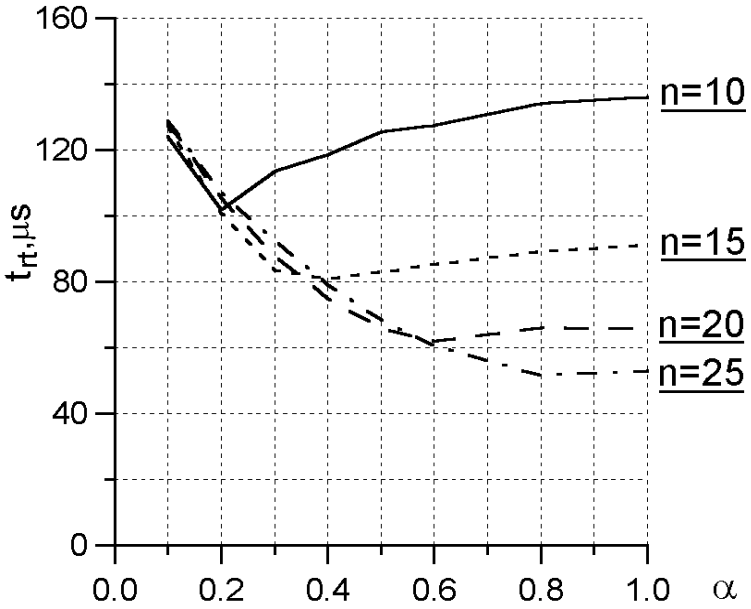

Figure 19: Dependence of the pulse rise time formed by a ladder PFN on n and α.

In choosing the mismatch coefficient α and the number of cells n, the effect of these parameters on the losses in elements of the ladder PFN, like capacitors and cell coils, should be taken into account.

In accordance with [21], the relative value of total losses in the cell inductances of the ladder PFN come to

$$\frac{W_{rL}(\alpha)}{W_{tot}} = \frac{r_L(\alpha)}{2R_{load}}(n+1), \tag{3}$$

where r_L is a cell coil resistance, $W_{tot} = \int_0^{t_p} u_p(t) i_p(t) dt$ is the pulse energy on the load. As is seen from this expression, the nature of the dependence $W_{rL}(\alpha)$ is the same as the nature of the dependence $r_L(\alpha)$. Setting the copper cross section of the coil winding to be constant, the resistance r_L increases with the increase of α because $r_L \sim w \sim \sqrt{L} \sim \sqrt{\alpha/n}$. In above w is the number of coil turns, L is the coil inductance. Hence, according to relation (3) $W_{rL}/W_{tot} \sim \sqrt{\alpha n}$.

The relation between the operating current through the capacitors of i-th cell I_{Ci} and operating current through the load I_{load} in the ladder PFN is calculated as follows [21]:

$$\left(\frac{I_{Ci}}{I_{load}}\right)^2 = \frac{2}{\pi n}, \quad i = 2, ..., n-1 \tag{4}$$

$$\left(\frac{I_{C1}}{I_{load}}\right)^2 = \frac{17}{8\pi n}, \quad \left(\frac{I_{Cn}}{I_{load}}\right)^2 = \frac{8}{3\pi n}. \tag{5}$$

Therefore the relative losses in the cell capacitors of the ladder PFN are equal to

$$\frac{W_{rC}}{W_{tot}} = \frac{r_C}{R_{load}}\left(\frac{2(n-2)}{\pi n} + \frac{17}{8\pi n} + \frac{8}{3\pi n}\right) \tag{6}$$

Here r_C is equivalent resistance of capacitor losses (in the series circuit of the capacitor substitution) which can be presented by the following expression

$$r_C = \frac{tg\delta}{2\pi f C} = \frac{n\alpha R_{load} tg\delta}{\pi f t_{pC}}, \tag{7}$$

where $tg\delta$ is the dissipation factor of the PFN capacitors, $f = 1/2t_{pC}$ is the equivalent operation frequency of capacitors (t_{pC} is the current pulse duration in the capacitor). As the numerical analysis shows f weakly depends on n (if $\alpha < 0.4$) and increases approximately as $\sqrt{\alpha}$ when α increases. Thus, it follows from (4÷7) that the losses in the PFN capacitors increase to some extent when α increases and linearly increase when n increases (under the condition that the dissipation factor is constant in the given range of frequency).

From the said above, it follows that it is preferential to use the PFN with a small impedance and cell number from the viewpoint of the losses decrease.

From (4) and (5) it follows that the current load over the capacitors (the relation between the operating current through the capacitor and his capacitance [A/μF]) of each of the ladder PFN cell depends on n as $\sim \sqrt{n}$ and depends on α as $\sim \alpha$.

According to (2) the inductance of PFN coils linearly increases with α, which means that their dimensions have also to be increased. This complicates the design of a PFN. The voltage drop on the PFN capacitors can be calculated with a good accuracy by the formula: $\frac{\Delta U_{pfn}}{U_{pfn}(0)} = \frac{2\alpha}{1+\alpha}$. From here it follows that the growth of α leads to an increase in the voltage drop on the capacitors, and hence, to a more intensive operation mode of the capacitors.

As is seen further, the charge device has a larger efficiency in the case of a partial discharge of PFN capacitors than in the case of its total discharge. It counts in favor of small α because small α corresponds to a small PFN discharge.

In choosing the mismatch coefficient α, it is useful to take into account the possibility of modernization of the existing B-modulator, that is, the use of the existing B-modulator elements such as the IGBT switch, power supply, capacitors of the main storage capacitor. In this case [4] the voltage of the charge power supply $U_{PFN}(0) = 10.6$ kV, the voltage over the primary PT winding $U_{load} = U_{kl}/k_{PT} = 9.17$ kV and the current recalculated to the primary PT winding $I_{load} = 1560$ A. The value of α comes to

$$\alpha = \frac{\rho}{R_{load}} = \frac{U_{PFN}(0) - U_{load}}{I_{load}} = 0.156.$$

Thus, using this line of reasoning it is worthwhile to take the PFN with $\alpha = 0.156$ as an operating version for the ladder PFN.

As was shown above, from the point of view of minimizing the losses in the coils and PFN capacitors, as well as for the sake of decreasing the current load on the PFN capacitors, the minimum number of cells should be chosen for PFN. The pulse rise time does not grow with the reduction of n down to $n \approx 10$. Further we shall consider the version of the ladder PFN with $n = 11$. The number n is determined by the given cell capacitance $C = 75$ μF (three capacitors each of 25 μF as in the main capacitor bank of the B-modulator), by PFN impedance $\rho = \alpha R_{load} \approx 0.91$ Ohm and pulse duration t_p in accordance with equation (2). In order to obtain the pulse flat top duration $t_{top} = 1.3$ ms, the cell inductance should be equal to 63.3 μH, the PFN impedance $\rho = 0.92$ Ohm and $\alpha = 0.156$.

Further we shall analyze the charging process in the ladder PFN in detail as well as the processes in the PFN in the case of a load breakdown.

4.3.2 Suppression of the oscillations in PFN after the pulse generation

Because the mismatched PFN discharges not completely and its pulse fall time is formed by a switch, the cell capacitors of the ladder PFN are discharged to different voltages after the pulse end [17]. This causes an oscillation process and additional losses in the circuit elements after the pulse generation.

The duration and intensity of these oscillations in the ladder PFN after the pulse can be decreased by increasing the number n of cells, decreasing of α, using a charge of the PFN cells through the diode stack (diodes D_c) and using diodes (D_{cell}) connected in series with the PFN coils [22] (see Fig. 20).

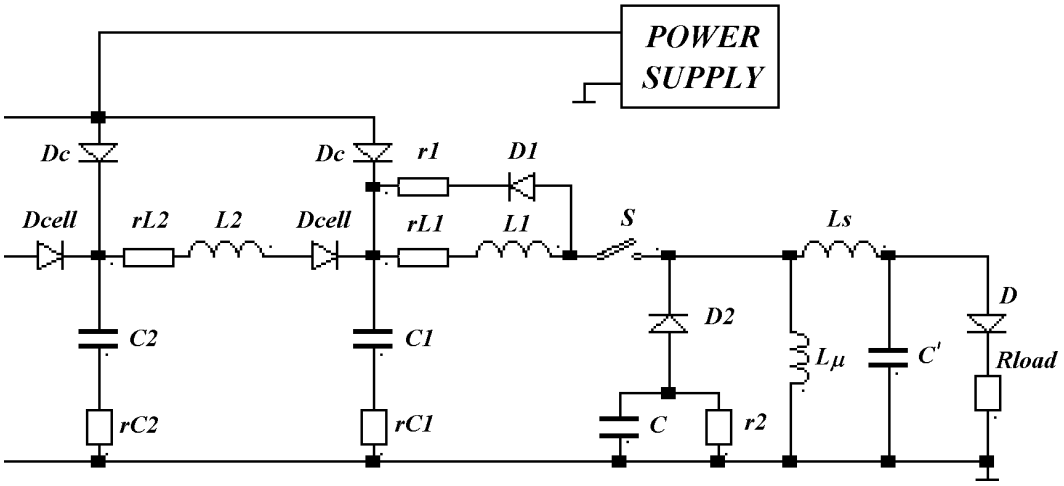

Figure 20: Circuit for simulation the oscillations in ladder PFN after the pulse generation.

In order to illustrate the possibilities to suppress oscillations in the PFN after the pulse with the help of the diode stack and diodes D_{cell}, Fig. 21 demonstrates the shapes of currents through the capacitance C_6 of the PFN (not shown on Fig. 20) with using diode stack and without them for different numbers of diodes D_{cell} in both cases. The oscillations in the PFN are damped in a quicker manner with using the diode stack, when diodes D_c are set to each PFN cell (see Fig. 21).

This figure also shown that the oscillations after the pulse can be suppressed more radically if the diodes D_{cell} are connected in series with the PFN coils (see Fig. 20). Even a few diodes at the beginning of the network essentially suppress the oscillation process because just the capacitors of the first cells are discharged to a lesser extent than the others by the pulse end and cause the oscillations.

Numerical simulation of this scheme were carried with using diode stack and without them for different numbers of diodes D_{cell} from 0 up to 8 in both case. The resistance of the coils r_L and angle of losses of the capacitors $tg\delta$ were chosen such that the losses in this elements during one pulse should not exceed 0.5% of the value W_{tot}, which approximately corresponds to actual loss values.

In the Table 4 $n_{D_{cell}}$ denotes the number of diodes D_{cell}; W_{rL} and W_{rC} denotes the loss in the PFN coils and capacitors within the pulse ($t = 0 \div t_p$); W'_{rL} and W'_{rC} denotes the energy loss in the PFN coils and capacitors after the pulse ($t = t_p \div 200$ ms) (W'_{rL} does not include the energy stored in the first coil within the pulse ($W_{rL1}/W_{tot} = 0.3\%$) and the energy dissipated in the resistor R_1 after the pulse); I_{Cmax} denotes the maximum effective current through the PFN cell capacitors without regard for oscillation after the pulse; $I_{C\Sigma max}$ denotes the maximum of the effective currents through the PFN cell capacitors with regard to the oscillations after the pulse; W_{Dcell} denotes the energy losses in diodes D_{cell} at a voltage drop of 2 V across each device.

In accordance with the data obtained (see Fig. 21 and Table 4), to decrease the current load on the PFN capacitors, the number of diodes D_{cell} is to be no less than $6 \div 8$. The diode stack in

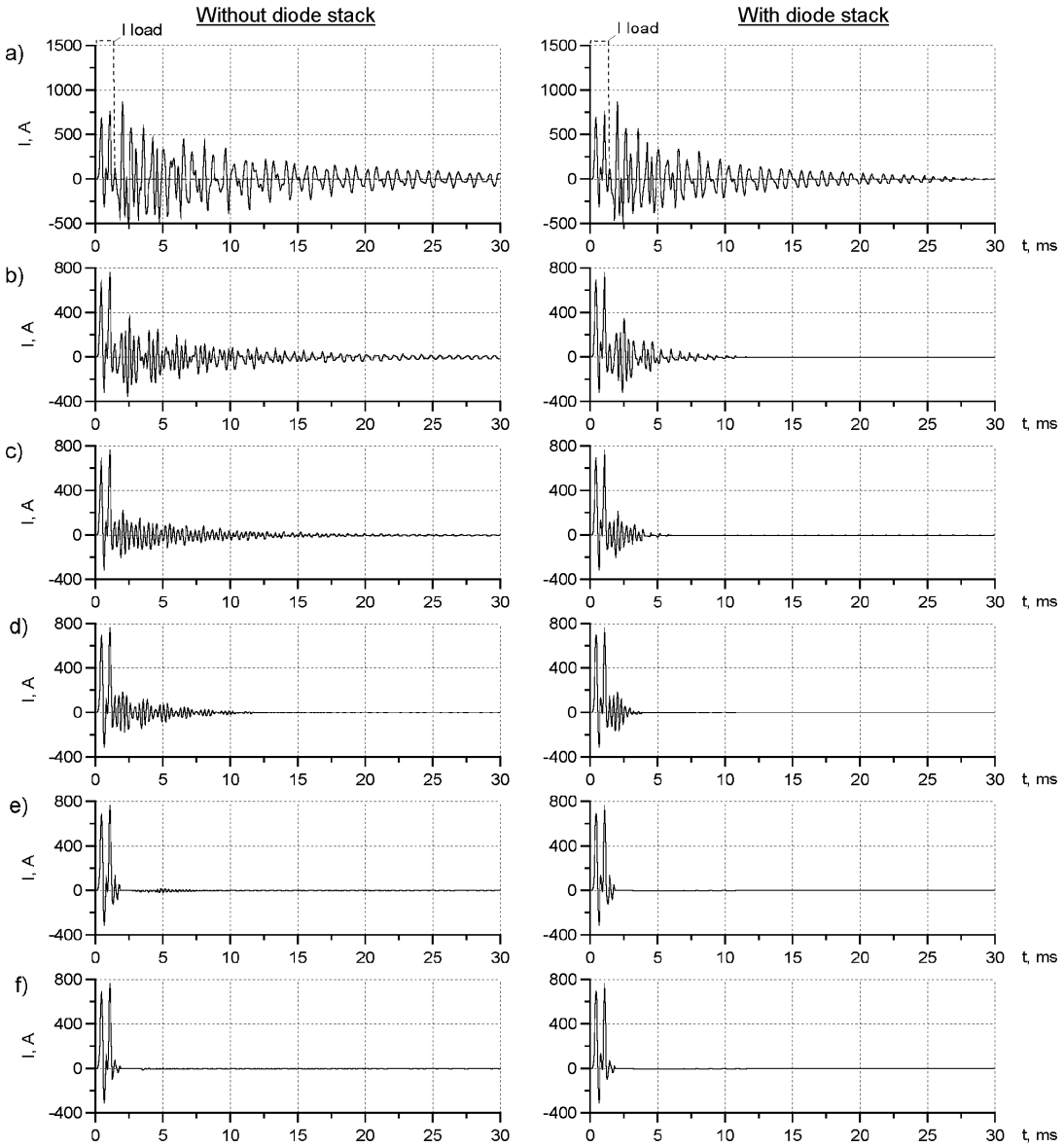

Figure 21: Current through the capacitor C_6 of the ladder PFN ($n = 11$, $\alpha = 0.156$) in the case of charging the PFN cells with a diode stack and without it. a) $n_{D_{cell}} = 0$; b) $n_{D_{cell}} = 1$; c) $n_{D_{cell}} = 2$; d) $n_{D_{cell}} = 4$; e) $n_{D_{cell}} = 6$; f) $n_{D_{cell}} = 8$.

Table 4: Effective currents through the ladder PFN capacitors and the losses in the PFN elements ($\alpha = 0.156$ and $n = 11$) in the case of charging with a diode stack and without it and for different number of diodes D_{cell} connected in series with network cells.

	Without diode stack						With diode stack					
n_{Dcell}	0	1	2	4	6	8	0	1	2	4	6	8
$I_{C\Sigma max}$,A	109	82	47	45.6	36.3	31	96.3	49	41	36.4	33.5	31
$I_{C\Sigma max}/I_{Cmax}$	3.57	2.7	1.54	1.49	1.19	1.02	3.15	1.6	1.34	1.19	1.1	1.02
W'_{rl}/W_{rl},%	104	7.2	1.2	0.43	0.34	0.3	64	2.5	0.4	0.04	0.03	0.02
W'_{rc}/W_{rc},%	480	64	21	4.3	1.7	0.35	328	32	8	2.7	0.9	0.2
W_{Dcell}/W_{tot},%	0	0.02	0.04	0.07	0.093	0.1	0	0.02	0.04	0.07	0.093	0.1

this case does not affect the charging process, therefore it can be ruled out in order to simplify the circuit. An advantage of the large number of diodes D_{cell} due to their presence in the majority of cells of the ladder PFN, the oscillation process is reduced in the circuit during the klystron breakdown and switching PFN off the load. Thus, it is possible to take the number of diodes D_{cell} to be equal to 10. The effective current through the diodes does not exceed 130 A and the back voltage comes to 1.4 kV.

4.3.3 Breakdown of the Load

The energy released in the klystron at the breakdown should be $\leq$ 20 J (see SoW). If the breakdown occurs in the case of the mismatched ladder PFN, the protection system used in the B-modulator can be partially applied [3, 4]. The IGBT switch disconnects the primary winding from the capacitors bank at a breakdown. The damping circuit (Fig. 14) which is in parallel with the PT primary winding absorbs the energy stored in the PT leakage inductance (L_s) and magnetization inductance (L_μ), and restricts the voltage over the PT primary winding down to 1600 V. In the case of abnormal work (breakdown) of the main IGBT switch, there is a possibility of additional protection of the klystron.

In this case the BACK UP switch comes into action and energy storages (the main storage capacitor in B-modulator or the first cell in the ladder PFN) are short-circuited. Each transistor of the BACK UP switch is protected with a varistor connected in parallel and which restricts the voltage over each transistor down to 480 V. Since the klystron protection in the case of a breakdown is one and the same in the circuits considered, the shape of the arc current and the energy released in the klystron do not differ.

Two operation modes of the protection circuit are possible in the case of a breakdown. They are:

a) Normal switch-off of the IGBT switch;

b) The IGBT switch is broken down, the BACK UP switch and the circuit which short-circuited the PFN capacitance come into action.

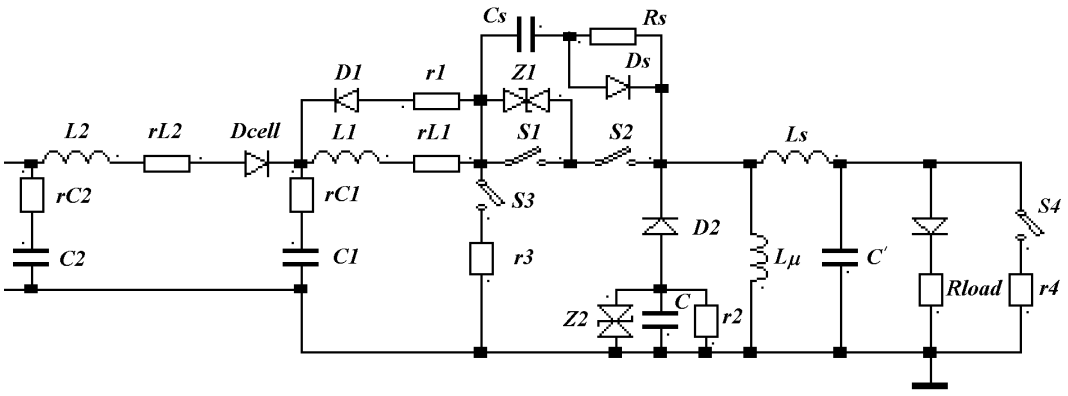

Figure 22: Design circuit of the ladder PFN ($n = 11$, $\alpha = 0.156$) at the load breakdown.

The breakdown processes in the ladder PFN are simulated by the circuit given in Fig. 22 for the ladder PFN at $\alpha = 0.156$ and $n = 11$. Fig. 23a presents the voltage and current pulse shapes in the circuit elements at the load breakdown within 400 μs after the pulse is applied when the main switch (S_2 in Fig. 22) is normally switched-off. Fig. 23b presents the same dependences at the breakdown of the main switch and when BACK UP switch (S_1 in Fig. 22) switches off and crowbar (S_3 in Fig. 22) switches on. In practice, there are no oscillations in the PFN elements after the pulse because of the diodes D_{cell}, when the main switch is normally switched off. In this case, the maximum back voltage over the diodes does not exceed 1.4 kV. The maximum voltage

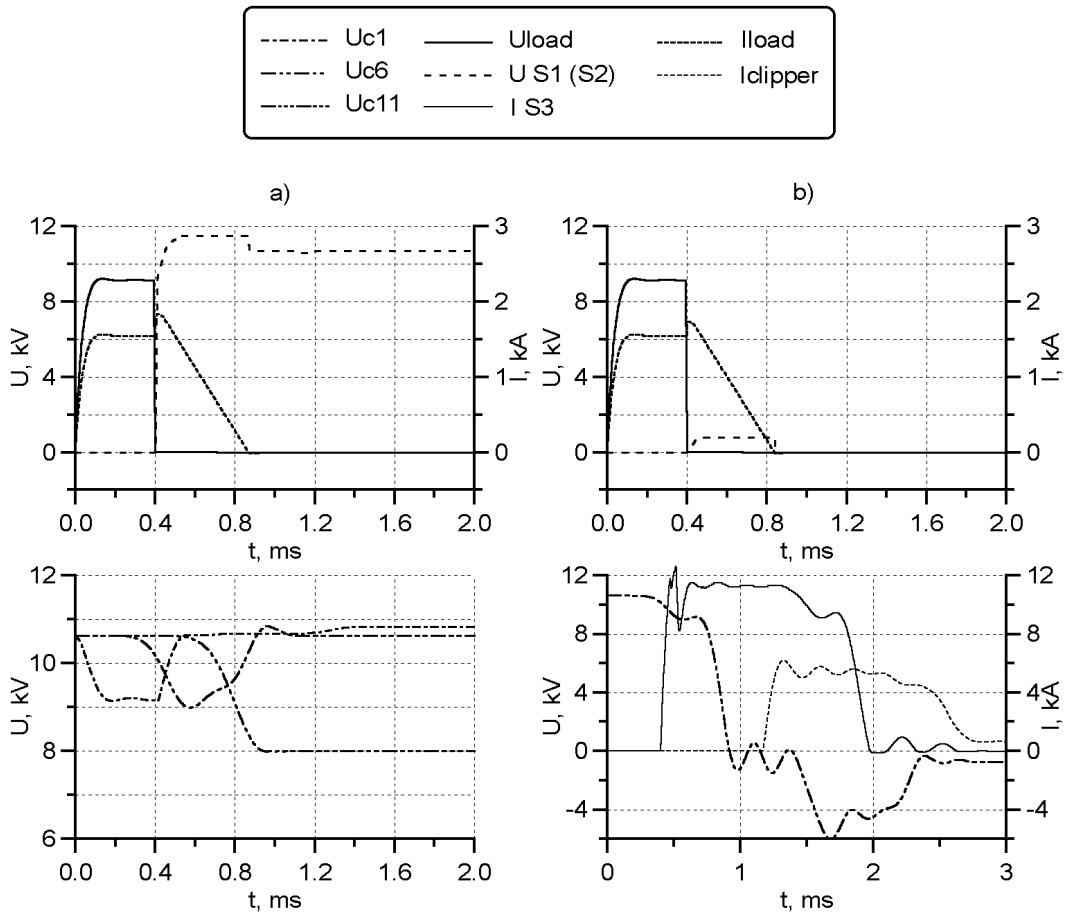

Figure 23: The transient processes in the ladder PFN elements ($n = 11$, $\alpha = 0.156$) at the load breakdown when the IGBT switch normally comes into operation (a) and in the case of a switch breakdown and an abnormal short-circuit of the PFN (b).

over the IGBT switch in the case (a) does not exceed the value of 12.5 kV proposed by designers in [4], that are, 925 V for each transistor (3 transistors of the BACK UP switch are working in a half–voltage mode). The rate of the current increase through the transistor switch is restricted with the PT leakage inductance L_s and the inductance of the PFN first cell $L_1 = 50$ μH. The rate comes to approximately 40 A/μs. Then if there is a delay in the main IGBT switch break-off of approximately 5 μs, the current through it does not exceed approximately 1.8 kA, which lies within the tolerable value for this IGBT switch.

In the case (b), the back voltage of an amplitude of 60% of the PFN charging voltage arises when the PFN was short-circuited. The amplitudes of the currents through the capacitors increase by a factor of approximately $5.5 \div 8$ as compared to the operating mode. The maximum current equal approximately to 9 kA comes through the capacitors of the first PFN cell (it corresponds to approximately 2.2 kA through one capacitor). This value does not exceed the current value through each of the 56 capacitors of the main storage capacitor of the B-modulator in case of its abrupt discharge of 130 kA/56 $\approx$ 2.3 kA. The current amplitude through the diodes D_{cell} is determined by the charging voltage and the PFN wave impedance and does not exceed 13 kA. The back voltage over these diodes does not exceed 1.4 kV either.

In conclusion, we should note that there are advantages of the PF on mismatched ladder PFN which allow to use it instead of the B-modulator. They are as follows:

- The PFN circuit is simplified because there is no BOUNCER circuit.
- The stored energy in the PFN is less than in the main storage capacitor in the B-modulator.
- A relatively low current of the abnormal PFN discharge makes it possible to design a short-circuiting semi-conductor switch allowing to simplify the crowbar operation in comparison with the dangerous of mercury ignitron in the case of the B-modulator.
- The efficiency of PF based on the ladder PFN increase because there is no restricting resistor r.

5 Feedline (FL)

5.1 General Properties of a Cables as the FL

In compliance with SoW a 3 km feedline (FL) between the modulator and the klystron pulse transformer should be designed. For the FL one can use coaxial, symmetrical cables, and various combinations of direct and reverse wires.

The coaxial cable has by its design one important advantage. Since both the magnetic and electric fields of the coaxial pair are concentrated inside of it, the coaxial cable induces only minimum noise onto neighboring circuits (low radiation effect).

The losses in the FL should not exceed 2% of the energy transmitted through this line (see SoW). This makes it easy to calculate what cross section the conductor should have to meet this condition. The role of the load is played by the klystron resistance calculated with respect to the primary winding of the PT $R_{load} = 5.88$ Ohm.

The resistance of the cable with no allowance for the skin effect

$$R_{cbl} = 2R_0,$$

where $R_0 = \dfrac{\rho \cdot l}{S_w}$ is the resistance of the cable conductors conducting the current in one direction, S_w is the cross section of the wires, ρ is the specific resistance of the conductor material, l is the feedline length. Hence,

$$S_w = \frac{2\rho \cdot l}{R_{cbl}}.$$

In view that the maximum value of $R_{cbl} = R_{load} \cdot 0.02 = 0.118$ Ohm, $l = l_{av} = 1700$ m, and for the copper $\rho = 0.0175$ Ohm·mm^2/m, we obtain $S_w = 500$ mm^2.

That is, in order to meet the requirements on the losses for a FL of middle length, there will be required the following mass of copper $m = 2 \cdot S_w \cdot l_{av} \cdot \rho_v \approx 15.3$ tones, where $\rho_v = 8.9 \cdot 10^{-3}$ g/mm^3 is the copper density.

Similarly for $l = l_{max} = 3000$ m $S_w = 882$ mm^2 we have $m \approx 23.6$ tones.

It requires a big amount of copper for one modulator. Since copper is a rather expensive material, one should compromise between the expenses for the copper and for the electric energy.

5.1.1 Pulse shape distortion during transmission along FL

The distortion of a pulse transmitted through the long FL is susceptible to the following factors:

1. Losses in the cable.
2. Wave impedance of FL ρ.
3. Time of FL delay t_d.

When the pulse is transmitted over a FL its shape is distorted due to the losses in metal, dielectric losses in the insulation, and the losses bound up with ionization processes. The ionization processes are basically caused by occluded air. With modern high – voltage coaxial cables with solid insulation one can neglect the impact of ionization processes on the pulse rise time distortion. The dielectric losses in the insulation for the cables with polyethylene insulation at frequencies up to 50 MHz (pulse rise time $\geq$ 10 ns) do not exceed $3 \div 5\%$ of the losses in metal [27], therefore for the case under consideration one can neglect the losses in the dielectric. The bulk losses occur in metal and determine the pulse rise time distortion. These distortions depend upon the presence of skin effect and proximity effect for the coaxial and symmetrical cables.

The depth penetration of sinusoidal current into copper conductor is defined [30] as $\theta = 6.6/\sqrt{f}$ [cm], where f is the signal frequency [Hz]. In accordance with [31], to determine the skin depth of the pulse current it can be used a correlation between the sinusoidal signal frequency f and rectangular pulse duration τ such as $f \approx 1/(2\tau)$, then the dependence between θ and pulse time can be defined as $\theta = 6.6\sqrt{2\tau}$. For the pulse with rise time t_{rt} the corresponding frequency is $f = \dfrac{1}{2(2t_{rt})}$. Thus, to obtain the pulse rise time no more than 100 μs it is necessary to take the conductor radius r or thickness t no larger than θ, thus we must have $r = t \leq 1.4$ mm.

In order to decrease the skin-effect for large cross section, it is suitable to make an inner cable conductor as a number of insulated wires of radius $r \leq 1.4$ mm twisted together.

From technological considerations, an outer conductor is made as a braid of non-insulated wires with diameter of $0.2 \div 0.3$ mm [30]. In this case, taking into account the twist coefficient k_1 and braid coefficient k_2 [30], the total weight of copper increases by a factor of $(k_1 + k_2)/2$. Again, the outer conductor thickness does not exceed θ or $t \leq 1.4$ mm in order to obtain $t_{rt} = 100$ μs.

For a symmetrical cable it is necessary to take into account the proximity effect [30]. In this case, both conductors of symmetric cable such as back and forward are to be manufactured of insulated wires of small radius ($r = \theta/2 \leq 0.7$ mm for $t_{rt} = 100$ μs).

The cable wave impedance and delay time has affect on the pulse rise and fall times duration, and they will be taken into account in the design of a real power supply systems.

In view of the above the following conclusions can be made:

1. In order to obtain the pulse rise time of about 100 μs at the output of FL it seems reasonable to make the cable conductors of insulated wires of radius not exceeding 1.4 mm;

2. In order to obtain the required by SoW value of losses in the FL of a middle length, it is expedient to use a cable with a total cross section of both direct and reverse conductors of no less than 500 mm^2;

3. The coaxial cable is more preferable as a feedline than a symmetrical one.

5.2 The inclusion of the FL effect in the actual PFs

In addition to a distortion of the pulse shape caused by the skin effect, we should take into account a distortion of the pulse shape caused by the FL operation in the actual PFs (it is assumed that the thickness of the back and forward cables are taken so that to provide a pulse rise time not exceeding 100 μs).

As is seen earlier, the following decisions of the PF for supplying klystron of 10 MW are more preferable:

1. Partial capacitance discharge circuit (B-modulator).

2. Mismatched ladder PFN circuit.

5.2.1 Partial capacitance discharge circuit (B-modulator)

Let us consider the effect of FL in the B-modulator circuit (see Fig. 14). The calculated circuit of this power supply are shown in Fig. 24. The parameters of this circuit are: $C_1 = 1400$ μF,

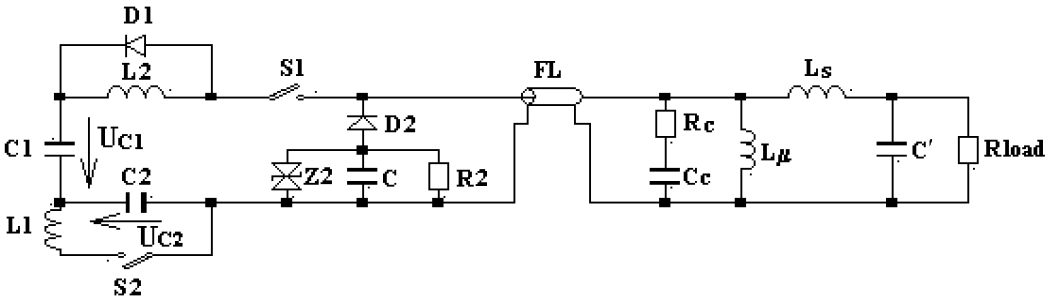

Figure 24: Calculated circuit of the klystron power supply with the B-modulator and the FL, located before the PT.

$U_{C_1}(0) = 10.1$ kV, $C_2 = 2000$ μF, $U_{C_2}(0) = 1.4$ kV, $L_1 = 330$ μH, $R_{load} = 5.88$ Ohm is the klystron equivalent resistance, $R_2 = 160$ Ohm, $C = 100$ μF. PT parameters: $L_s = 190$ μH is PT leakage inductance, $L_\mu = 1.13$ H is PT magnetization inductance, $C' = 120$ nF is PT and klystron capacitance. $L_2 = 50$ μH is additional inductance. All the values are referred to the primary circuit. The time delay corresponding to 3000 m long FL with polyethylene insulation is $t_d = 15$ μs. Switch S_2 turn on without delay and turn off after pulse ending, switch S_1 turn on with the time delay about 750 μs and turn off through $t_p = 1.4$ ms.

The pulse shapes on the load, as a factor of R_{load}/ρ, calculated by scheme (Fig. 24) are shown on Fig. 25 and Fig. 26 (without and with regard for the effect of correcting circuit R_cC_c, correspondingly). A comparison between Fig. 25 and Fig. 26 shows that the high-frequency

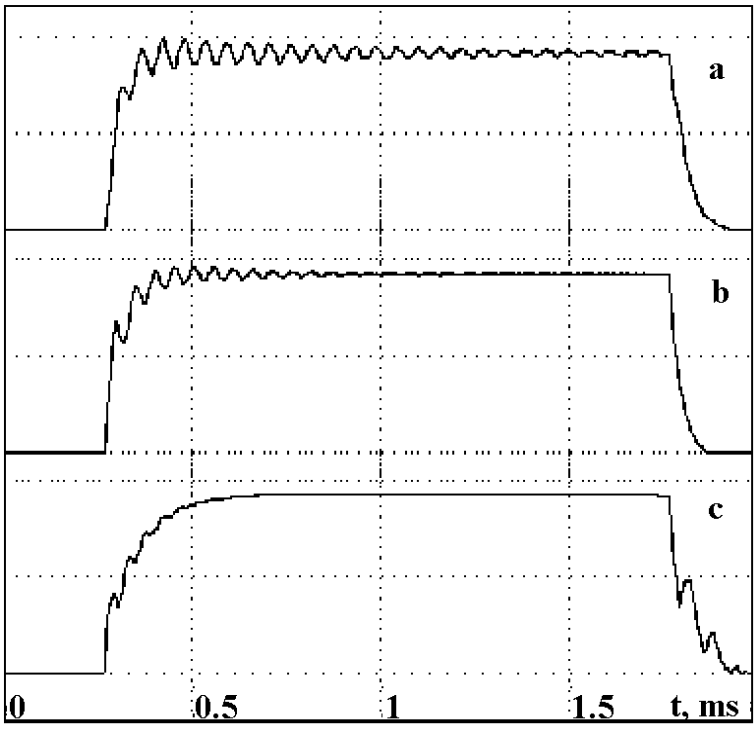

Figure 25: Voltage pulse shape on the load without the correcting R_cC_c-circuit as a factor of R_{load}/ρ. $t_d = 15$ μs. a) – $R_{load}/\rho = 3$, b) – $R_{load}/\rho = 1$, c) – $R_{load}/\rho = 0.3$. Scale is 5 kV/div. (B–modulator).

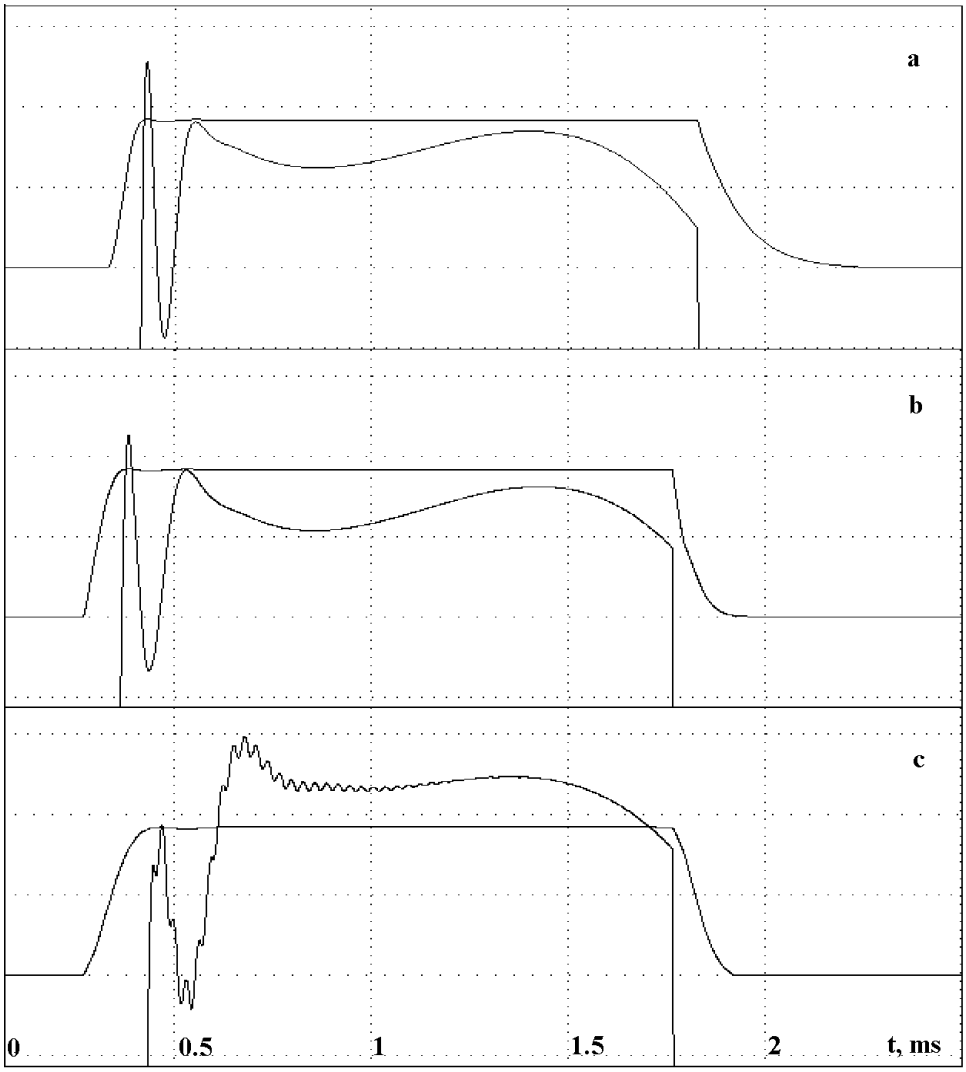

Figure 26: Voltage pulse shape on the load as a factor of R_{load}/ρ with the correcting R_cC_c-circuit. $t_d = 15$ μs. a) – $R_{load}/\rho = 3$, b) – $R_{load}/\rho = 1$, c) – $R_{load}/\rho = 0.3$. Scale is 5 kV/div and enlarged to 50 V/div. (B–modulator).

oscillations at the pulse rise time and the pulse flat top caused by the effect of FL and L_s are cleared with the correcting circuit R_cC_c switched after the FL in parallel with the PT. The optimal values of R_c, C_c used for calculations and the data on the losses in the circuit are listed in Table 5. Here W_{R_c} is the losses in resistance R_c, W_{rt} and W_f are the part of pulse energy dissipated in the load during the pulse rise and fall times, correspondingly, $W_\Sigma = W_{rt}+W_f+W_{R_c}$ is the losses.

In the best version of RC-circuit the parameters of the FL wave impedance, the FL length and the R_cC_c-circuit are chosen to obtain the instability in the pulse flat top not exceeding $\pm 1\%$ and minimum energy losses in the circuit elements. As is seen from the numerical simulations (see Table 5), the optimum FL wave impedance which requires these conditions is $\rho = R_{load} \approx 6$ Ohm. The numerical simulations have been carried out for the maximum FL length of 3000 m. For reference, Table 6 lists the data on losses in the B-modulator circuit with the FL length of 1700 m and $\rho = R_{load} \sim 6$ Ohm.

A comparison between Table 5 and Table 6 shows that for a long FL the losses on the pulse rise and fall times and in R_c become smaller in the case of B-modulator. This can be explain by the correction of pulse rise time at the expense of the FL length. Then larger is the FL length, than more readily the correction can be made (the value C_c is smaller).

Table 5: Losses in the B-modulator circuit with the FL length of 3000 m for the various R_{load}/ρ.

$\frac{R_{load}}{\rho}$	$\frac{W_{R_c}}{W_{tot}}$, %	$\frac{W_{rt}}{W_{tot}}$, %	$\frac{W_f}{W_{tot}}$, %	$\frac{W_\Sigma}{W_{tot}}$, %	t_{rt}, μs	R_c, Ohm	C_c, μF
3	2.6	2.6	3.8	9.0	89.5	1.8	12
1	1.8	3.6	1.9	7.3	105	2.7	7
0.3	0.7	5.7	3.2	9.6	175.5	1.4	7.5

Table 6: Data on losses in the B-modulator circuit with the the FL length of 1700 m and $\rho = R_{load} \sim 6$ Ohm.

$\frac{W_{R_c}}{W_{tot}}$, %	$\frac{W_{rt}}{W_{tot}}$, %	$\frac{W_f}{W_{tot}}$, %	$\frac{W_\Sigma}{W_{tot}}$, %	t_{rt}, μs	R_c, Ohm	C_c, μF
2.1	3.4	2.4	7.9	104	2	9.5

5.2.2 Mismatched ladder PFN circuit

Let us consider the effect of the FL on the voltage pulse shape on the load in the mismatched PFN circuit. The numerical simulation of the mismatched PFN circuit with FL have been carried out by the scheme in Fig. 27. They show that W_Σ does not depend in an explicit form on α within 0.1 and 0.5 and cells number in a range between $n = 11 \div 16$. Let us consider an operation of the mismatched PFN circuit with parameters $\alpha = 0.156$, $n = 11$ and FL length of 3000 m. Numerical simulations of this scheme (see Fig. 27) have been carried out with the following parameters: $L_1 = 50$ μH, $L_2 = L_3 = ... = L_{11} = 63.3$ μH are inductances of PFN cells, $C_2 = C_3 = ... = C_{11} = 75$ μF are capacitances of PFN cells, the first cell capacitance C_1 is corrected depending on FL length, $C = 100$ μF, $R1 = 0.5$ Ohm, $U_{Z2} = 1600$ V, $R2 = 30$ Ohm.

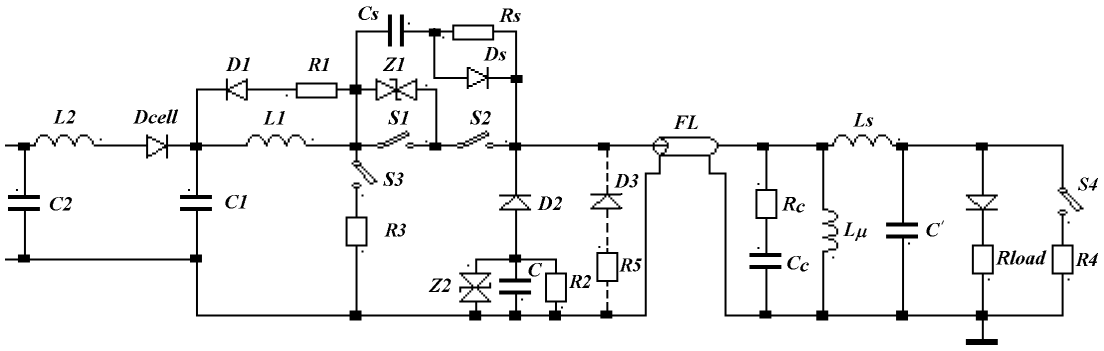

Figure 27: Calculated scheme of klystron power supply on mismatched ladder PFN with FL.

The voltage pulse shapes on the load of the mismatched PFN with FL without and with regard of the correcting R_cC_c circuit are presented on Fig. 28 a and b, correspondingly. The high-voltage oscillations are presented at the pulse rise time and flat top caused by the FL effect (Fig. 28 a). Their amplitude exceeds the admissible distortions on the pulse flat top ($\pm 1\%$). The oscillations can be reduced (see Fig. 28 b) by correcting circuit R_cC_c connected after the FL in parallel with the PT and the choice of parameters of the first PFN cells. From the numerical simulation it will be found the optimal parameters of circuit: $C_1 = 100$ μF, $C_c = 4.3$ μF, $R_c = 3.1$ Ohm, and $\rho = 7$ Ohm.

Table 7 gives the losses in the mismatched PFN circuit at different FL length. As is seen from Table 7, the values of W_Σ/W_{tot} do not differ more than 0.5% in the mismatched PFN circuit for the different FL length.

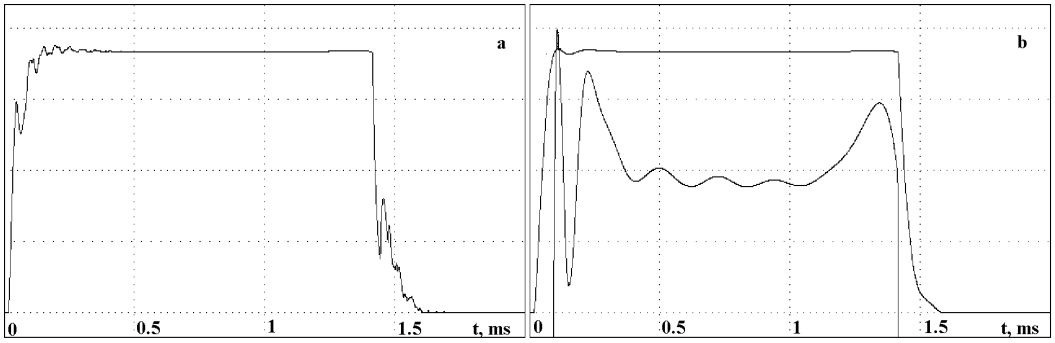

Figure 28: The curves for the voltage on the load for the mismatched ladder PFN ($\alpha = 0.156$, $n = 11$, FL length is 3000 m. Curve (a) is without the correcting circuit, curve (b) is with the correcting circuit. Scale is 2.5 kV/div and enlarged to 50 V/div.

Table 7: Losses in the mismatched ladder PFN circuit for different FL length and $\rho = 7$ Ohm

	$\frac{W_{R_c}}{W_{tot}}, \%$	$\frac{W_{rt}}{W_{tot}}, \%$	$\frac{W_f}{W_{tot}}, \%$	$\frac{W_\Sigma}{W_{tot}}, \%$	t_{rt}	R_c, Ohm	C_c, μF
$\alpha = 0.156, l = 3000$ m	1.2	2.6	1.8	5.6	81.5	3.1	4.3
$\alpha = 0.156, l = 1700$ m	1.2	2.3	1.9	5.4	76	2.2	5
$\alpha = 0.156, l = 50$ m	–	4.6	1.3	5.9	101.2	–	–

5.3 Possible versions of the FL

As a possible variants to stock-produced Russian-standard cables, the cables KVI-330, FKP, and RK-75-24-17 are proposed for the FL production. Table 8 lists the main parameters of these cables (see Fig. 29, 30). In this table d_c is the diameter of the wires making the conductor,

Table 8: Cable parameters

Type	d_c mm	d_0 mm	d mm	d_{sh} mm	D mm	D' mm	R_{cbl} Ohm/km	ρ Ohm
KVI-330	0.3	10.2	11.7	0.3	19.8	21	5.625	21
FKP-1/50	0.3	9	10.5	0.3	13.3	14.5	6.807	12
RK-75-24-17	3.6		3.6	0.3	24.7	26.9	3.524	75

d_0 is the inner diameter of the insulating core, d is the outer diameter of the conductor, d_{sh} is the diameter of the shield wires, D is the inner diameter of the shield, D' is the outer diameter of the shield, R_{cbl} is the total active resistance of the conductor and the shield, ρ is the wave impedance of the cable. As is seen from Table 8, all the presented cables have such a direct and reverse conductor thickness which allows to obtain at their output the pulse rise time not exceeding 100 μs (an exception is RK-75-24-17 cable with $d/2 = 1.8$ mm). At the same time, an active conductor resistance on the length of 1.7 km exceeds the permitted resistance 0.118 Ohm. As an example, to satisfy the demands on FL losses (2%), it is necessary to take 90 cables RK-75-24-17, connected in parallel.

On Fig. 29 it is suggested the cable design providing the losses within the range of 2% for FL of 1700 m length and $t_{rt} \leq 100$ μs. Here $d \approx 30$ mm is the outer diameter of the conductor, $D \approx 36$ mm is the insulation diameter or the inner diameter of the shield, $D' \approx 46$ mm is the outer diameter of the shield, $d_{sh_2} \approx 52$ mm is an additional grounding shield, $d_{coat} \approx 58$ mm is the

outer diameter of the cable coating. The wave impedance of this cable is $\rho \approx 7.4$ Ohm. The cable conductor is made of insulated wires with the diameter $d_c \leq 1.4$ mm. The braid of the cable shield is made of insulated wires with the diameter $d_{sh} \leq 1.4$ mm. Based on the above conductor cross section $S_w \sim 500$ mm^2 and having regard to the twist k_1 and braid k_2 coefficients, the required cross section of the conductor and shield make: $S_c = S_w \cdot k_1$, $S_{sh} = S_w \cdot k_2$. For $S_w = 500$ mm^2, $k_1 = k_2 = 1.15$ we obtain $S_c = S_{sh} = 575$ mm^2. Hence, the number of the conductor filaments makes $n_c = n_{sh} = \dfrac{S_c}{\pi d_c^2/4} = 732$. As is shown above, since $R_{load} = 5.88$ Ohm, then for obtaining the value of $t_{rt} \leq 100$ μs and the level of instability at the pulse flat top around $\pm 1\%$ of U_{kl}, the cable should have $\rho \approx 7$ Ohm. The thickness of the insulation (fluoroplastic, polyethylene or combined) at a voltage $U_{pr} = U_{kl}/K_{tr} \approx 10$ kV should make $\geq 2.5 \div 3$ mm.

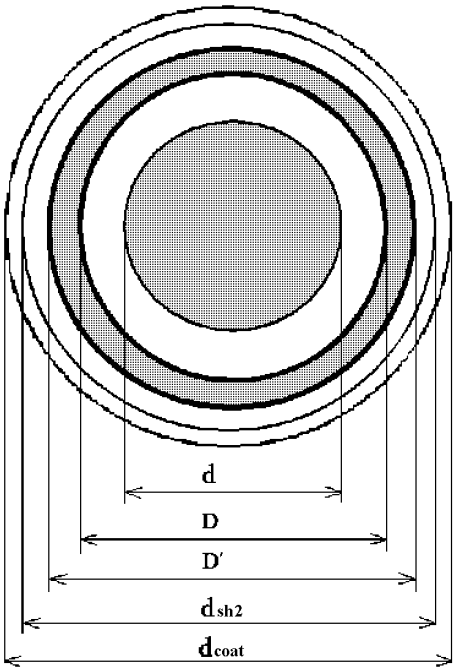

Figure 29: Cable construction answering the requirements of SoW (single cable).

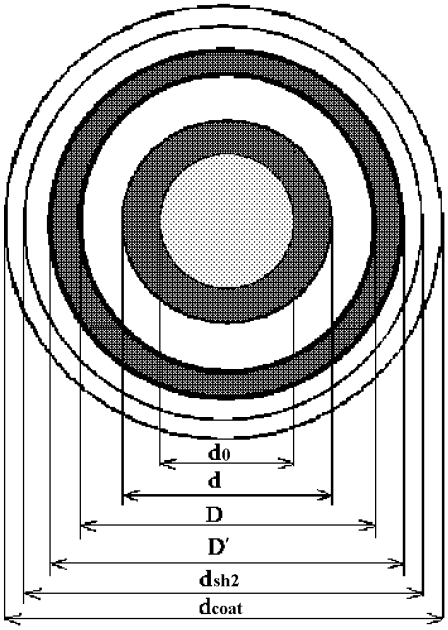

Figure 30: Cable construction with the low copper consumption (8% looses in the FL).

In view that the FL with the losses preserved at a level of 2% requires a large quantity of copper for the conductor, it seems reasonable to consider a variant of the FL with a higher level of losses but a lower copper consumption. Let us assume, for instance, that the losses in the cable should not exceed 8%, hence, the required copper cross section is reduced to one fourth, i.e. $S_c = S_{sh} = 575/4 = 144$ mm^2. In this case for obtaining the minimum wave impedance, the conductor and the shield should be made as the braids of insulated wires with $d_c = d_{sh} \leq 1.4$ mm. The conductor braid is applied to a polyethylene rod, its diameter being $d_0 \approx 25$ mm (see Fig. 30), $d \approx 29$ mm $D \approx 35$ mm, $D' \approx 38$ mm, $d_{sh2} \approx 44$ mm, $d_{coat} \approx 51$ mm. The wave impedance of this cable $\rho \approx 7.6$ Ohm. The thermal calculation has shown that the maximum effective current through such a cable is $I_{max} \approx 300$ A, the required effective current is $I_{eff} = I_{kl}\sqrt{\frac{t_p}{T}} = 130$ A, here $T = 1/f_{prr}$ is the period of pulses succession. The numerical calculations show that when using a cable with a 1/4 copper consumption, the power supply voltage should be increased by $\approx 10\%$ compared to the nominal one.

The using of litzendrat as a FL, in opinion of experts of Special Design Department of Cable Industry (SDDCI, Russia), is made difficult by the following reasons:

1. The litzendrat conductors should be twisted together so that all of them will be in identical conditions - each conductor should be placed alternatively at a braid surface and inside the braid. Otherwise the greater current will run through the conductors located at the braid surface.

2. The cable with insulated conductors will cost considerably higher than the cable with non-insulated conductors.

Therefore below the next version of a cable which consists of two braids (inner and outer) with a thickness of 1.4–2 mm made of non-insulated conductors with diameter of 0.3 mm (diameter is chosen on the basis of manufacturing considerations) is discussed (see Fig. 30). The inner braid is mounted on a core made of insulating material (polyethylene). The additional shield made as a braid allows to provide an electric safety and noise-free of the system. The dimensions of this cable with a losses in a middle length FL not more 2% are following: $d_0 = 80$ mm, $d_1 = 84$ mm, $D = 94$ mm, $D' = 98$ mm, $d_{sh2} = 102$ mm, $d_{coat} \sim 108$ mm. The wave impedance of this cable $\rho = 4.5$ Ohm.

But here are some problems in producing and servicing the cables of this large size.

Designers of SDDCI are ready to produce a cable with the following dimensions: $d_0 \approx 13$ mm, $d \approx 17$ mm, $D \approx 23$ mm, $D' \approx 26$ mm, $d_{sh2} \approx 30$ mm, $d_{coat} \approx 35$ mm, thickness of the additional shield is 0.6 mm. Wave impedance of such a cable $\rho = 13.5$ Ohm, and conductors cross-section without regard for filling factor $S_c \approx 70$ mm^2. Three such a cables connected in parallel may be used as a FL. In that case for the FL of length 1.7 km the losses at a level of $\approx 5.45\%$ will be provided, the wave impedance of the FL will be $\rho = 4.5$ Ohm.

5.4 Klystron breakdown with ability of FL

A klystron breakdown can be considered in the first approximation with the help of resistance R_4 and switch S_4 (Fig. 27). The resistance R_4, recalculated with respect to the primary PT winding, simulates the arc resistance at a klystron breakdown. The closure of the switch S_4 after a time interval $t_{S_4} = 400$ μs following the pulse beginning is equivalent to the klystron breakdown.

As is seen earlier, two operation modes of the protection circuit are possible at the klystron breakdown. They are:

a) Normal IGBT switch switch-off.

b) The main IGBT switch is broken down, the PFN capacitors are short circuited by the protection switch.

Let us consider the klystron breakdown at these regimes for the both modes.

Figure 31 presents the current and voltage curves for the PFN with FL at the klystron breakdown. The numerical simulation is done for the FL length of 3000 m, 1700 m and 50 m by the scheme in Fig. 27. As is seen from Fig. 31a, the voltage over the IGBT switch does not exceed 12.5 kV, this fact is in agreement with the requirements of the switch designers [4].

The total energy dissipated in the klystron at its breakdown can be calculated by energy dissipated in arc and spark stages of breakdown. For estimations the energy in the arc one can to use the following relation $W_{arc} = QU_{arc}$, where Q is a charge through klystron during the arc. Table 9 gives the data which features the energy in an arc in all cases given in Fig. 31 for the case of $U_{arc} = 200$ V.

Table 9: The energy losses in arc for the cases given in Fig. 31.

	a-1	a-2	a-3	b-1	b-2	b-3
W_{arc}, J	8.13	7.52	5.14	7.8	7	5

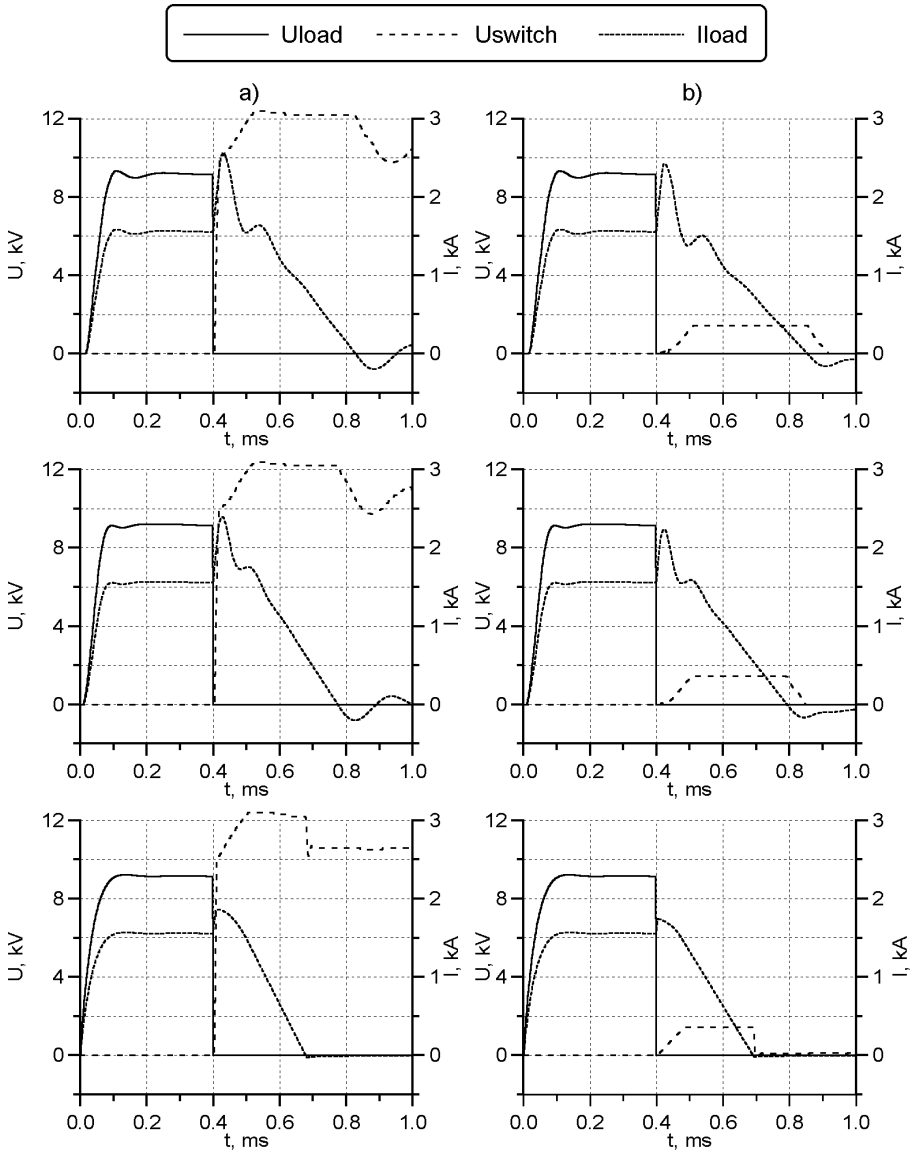

Figure 31: Current and voltage curves for the PFN with FL at the klystron breakdown. The main IGBT switch normally comes into operation (a), its breakdown and an abnormal PFN short-circuit (b). The FL length is 3000, 1700 and 50 m, correspondingly.

The energy losses in a spark W_{spark} can be estimated in the following way:

$$W_{spark} \sim W_{C_{kl}} + W_{C_{PT}} \approx 4.97 \text{ [J]},$$

where $W_{C_{kl}} = 0.3$ J is an energy stored in the klystron capacitance and $W_{C_{PT}} = 4.67$ J is an energy stored in the PT capacitance.

Thus, when it is used the power supply circuit for the klystron with FL between modulator and klystron PT, the total energy dissipated in the klystron does not exceed 20 J.

Below we can draw follow conclusions based on results of analyze of the FL:

1. It seems possible to realize the 10 MW klystron power supply using low voltage (10 kV) FL.
2. It will take a big amount of copper to produce such kind of FL.
4. The level of engineering experience for low voltage FL allows to begin its development immediately.

6 Magnetic coupling and nonlinear load. Pulse forming efficiency

As a result of the analysis, the following parameters of the mismatched ladder PFN elements are obtained:

- the number of the PFN cells is $n = 11$;
- the PFN cells inductance is $L_1 = 50$ μH, $L_2 = L_3 = ... = L_{11} = 63.3$ μH;
- the PFN cells capacitance is $C_2 = C_3 = ... = C_{11} = 75$ μF, the first cell capacitance is corrected in accordance with the feedline length.

As is seen in [16, 19], the magnetic coupling only between adjacent coils of the PFN cells allow to form rectangular pulses on the load so as it was in the case of the PFN without coupling. When the magnetic coupling is introduced between the adjacent PFN coils of the mutual inductance $k = M/L$, one and the same for each pair of PFN coils, the wave impedance of this line and the pulse forming duration can be defined in accordance with the following formula [20, 25, 26]:

$$\rho = \sqrt{\frac{L(1+2k)}{C}}, \quad t_p = 2n\sqrt{L(1+2k)C} \tag{8}$$

In accordance with [16, 19], the availability of a small coupling ($k = 0.1 \div 0.15$) decreases the oscillation amplitude on the flat top. When choosing the magnetic coupling coefficient k, the following facts should be taken into account:

1) the increase of k is beneficial in terms of a decrease in the overall PFN inductance;
2) a rather large k causes a distortion of the pulse flat top.

Numerical simulation of the mismatched PFN circuit with the magnetic coupling between the coils of adjacent cells (Fig. 32) shows, that to obtain the pulse flat top which meets the requirements of SoW, the coupling coefficient between all adjacent PFN coils, except for the first and second coils, is to be equal to $k = 0.15$ ($M_{1,2} = 0$). The PFN coils inductance is calculated in accordance with equation (8), the cells capacitances remain the same as in the case of the ladder PFN without coupling, that is

$$C_1 = 90 \div 115 \ \mu F, \quad C_2 = C_3 = ... = C_{11} = 75 \ \mu F \,,$$

$$L_1 = 50 \ \mu H, \quad L_2 = L_3 = ... = L_{11} = 46.5 \ \mu H \,.$$

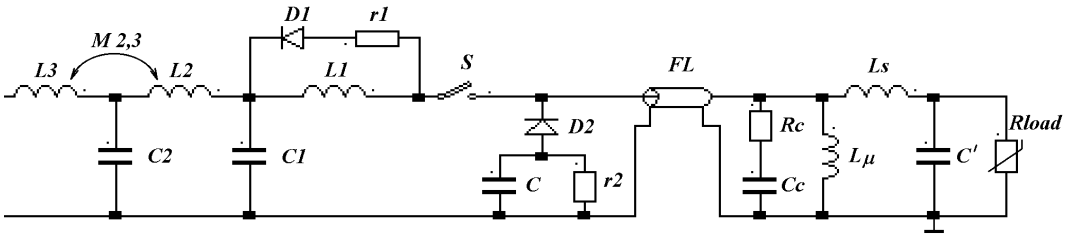

Figure 32: The design circuit for simulating PFN with the magnetic coupling with the FL and nonlinear load.

As is seen from above, the feedline requires a correction of the pulse shape with the help of an R_cC_c circuit (see Fig. 32). The volt-ampere characteristic (VAC) of the klystron are considered with allowance for the nonlinear resistance R_{load} with VAC calculated by the law of 3/2: $I_{load} = P \cdot U_{load}^{3/2}$. In the case of $U_{load} = 9.166$ kV and $I_{load} = 1560$ A, the coefficient P is equal to $1.78 \cdot 10^{-3}\text{A/V}^{3/2}$.

Fig. 33 presents the effect of the FL length on the pulse shape. Because the load is nonlinear, it is necessary to change the parameters of some PFN elements (such as correcting R_cC_c circuit, first cell capacitance C_1, and resistance r_1). Table 10 lists the parameters for the FL length of 50, 1700, and 3000 m. The energy loss in correcting elements within a pulse and the pulse rise time are listed in Table 11.

Table 10: Adjustable parameters of the circuit at the FL length equal to 50, 1700 and 3000 m.

l_{FL},m	R_c, Ohm	$_c, \mu$F	C_1, μF	r_1, Ohm
3000	3	5	115	1
1700	1.8	7	88	0.74
50	—	—	90	0.5

Table 11: Losses in the PFN circuit allowing for the load nonlinearity versus the FL length

l_{FL}, м	$\frac{W_{R_c}}{W_{tot}}$,%	$\frac{W_{rt}}{W_{tot}}$,%	$\frac{W_f}{W_{tot}}$,%	$\frac{W_{r1}}{W_{tot}}$,%	$\frac{W_\Sigma}{W_{tot}}$,%	W_{tot},kJ	t_{rt}, μs
3000	1.47	2.95	1.56	0.03	≈ 6	19.9	89.4
1700	1.58	2.67	2	0.1	≈ 6.4	19.9	89.3
50	—	6.2	1.2	0	≈ 7.4	20.08	136

The calculation shows that (see Table 11, Fig. 33) the pulse rise time increases by $20 \div 30\%$ in comparison with the linear load. This fact causes a decrease in the modulator efficiency.

The choice and calculations of main elements of the PF and its efficiency are given in the Appendix. The calculation results of the losses in the circuit elements with the FL length of 1700 m are listed in the following table:

PFN elements	895 W
including	
— PFN coils	370 W
— PFN capacitors	20 W
— diodes D_{cell}	100 W
— resistor r_1	405 W
IGBT switch	800 W
Correcting resistor R_c	1580 W
Undershoot circuit	420 W
PT windings and core	830 W
Feedline	2000 W
Total	6525 W

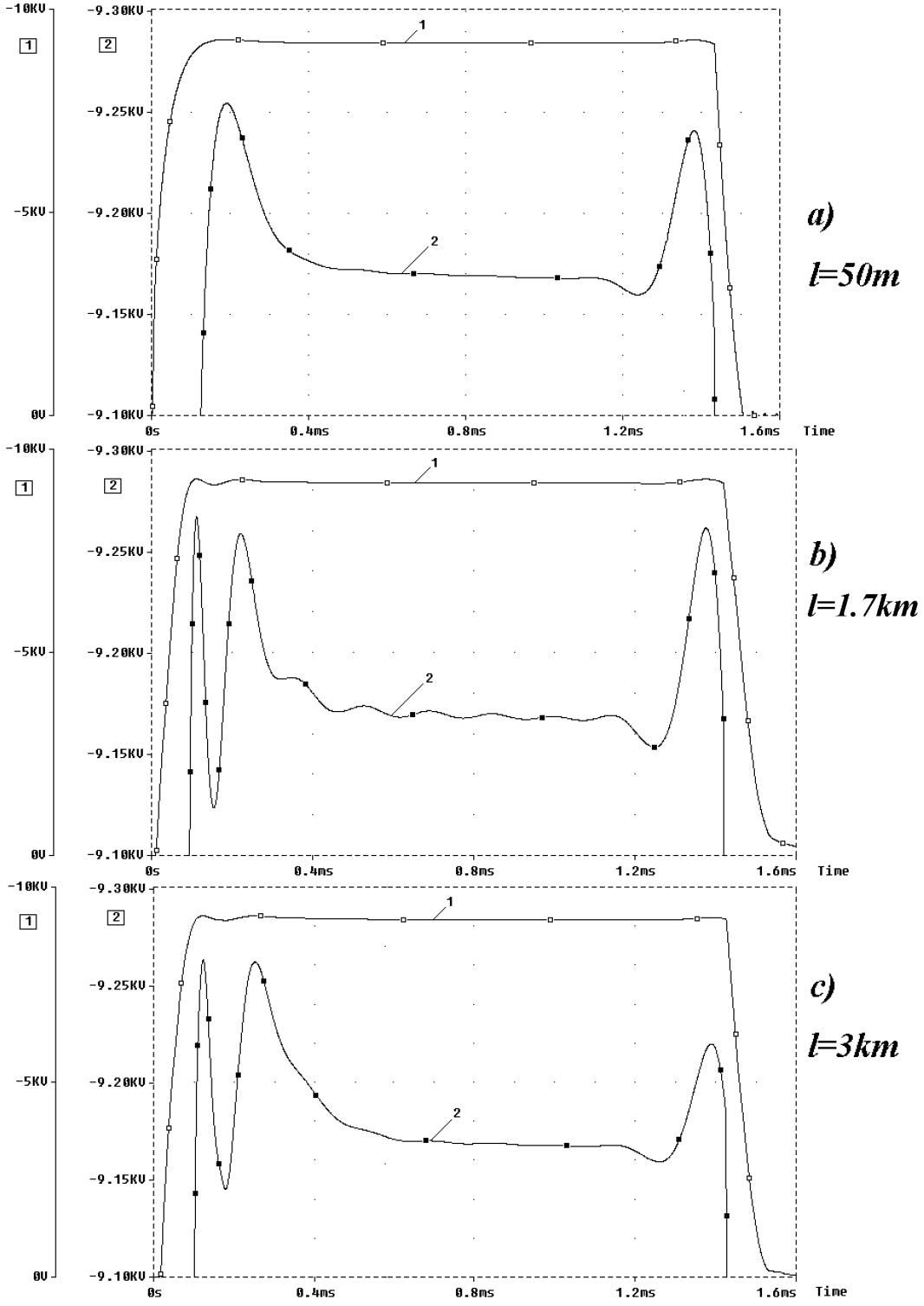

Figure 33: The pulse shape over the klystron at different FL lengths.

The power consumed by the klystron is equal to 19.9 kJ $\cdot$ 5 Hz = 99.5 kW, that consumed by the PFN is equal to $W_{PFN} = 99500 + 6525 = 106025$ W. Thus, the efficiency of the Pulse Former with a feedline $L_{FL} = 1700$ m and PT comes to

$$\eta = \frac{99500\ W}{106025\ W} \approx 0.94.$$

For the modulator with a feedline length of 50 m and 3000 m, the efficiency comes to $\eta = 100400$ [W]/103305 [W] = 0.97 and $\eta = 99500$ [W]/107375 [W] = 0.927, respectively.

If one takes into account that the "useful" energy is calculated in accordance with the pulse rise time and fall time, then the efficiency in accordance with Table 10 comes to:

$\eta = 0.9(0.92)$ at a FL length of 50 m;
$\eta = 0.895(0.9)$ at a FL length of 1700 m;
$\eta = 0.885(0.9)$ at a FL length of 3000 m.

The value of the efficiency given in the brackets was calculated under following conditions: values of W_{rt} and W_f were calculated with respect not to the flat top level, but to 0.98 of the pulse amplitude.

Fig. 34 presents the overall schematic of PFN based modulator.

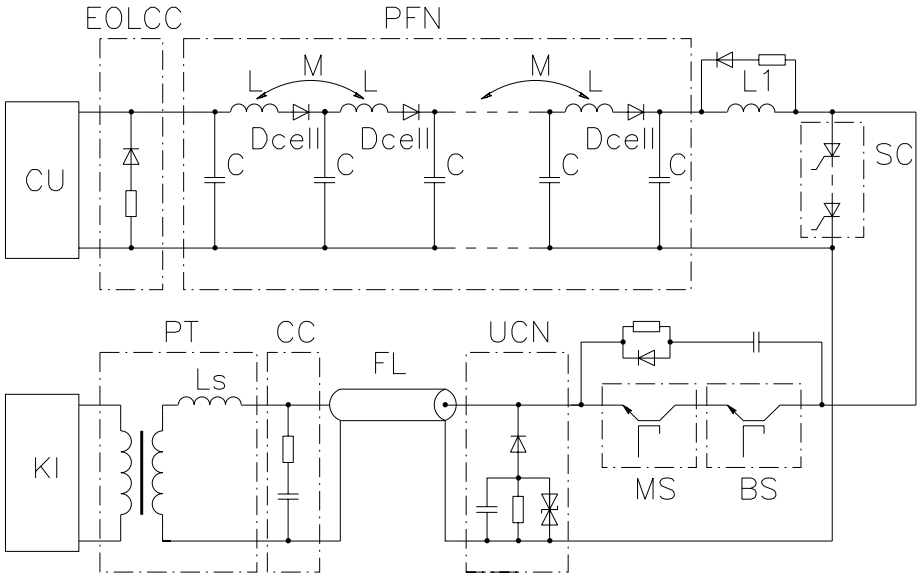

Figure 34: Overall schematic of PFN based modulator. CU - charge unit; PFN - mismatched pulse forming network with magnetic coupling; EOLCC - end of line clipper circuit; SC - semiconductor crowbar; MS - main IGBT switch; BS - back-up IGBT switch; FL - feedline; UCN - undershoot clipper network; CC - pulse correction circuit; PT - pulse transformer; Kl - klystron.

7 Constant Power Charge Device

7.1 Conceptual design of a constant power charge device

General requirements to the charge device are mentioned as follows:

- maximum efficiency;
- the mains should be loaded with a constant power with minimum ripple and phase distortions;
- no breaks in the power consumption during the operation cycle of the modulator;

- smooth control of voltage at the capacitance in a wide range (from zero to the maximum value);
- turn on of the modulators with a smooth transition to the operation regime;
- stabilization of the charge voltage;
- variation of the repetition rate of the modulator operation cycles from fractions of a Hz up to 5 Hz while preserving the condition of constant power consumption from the mains;
- obtain a maximum power factor of the rectifier, feeding the charge device by both decreasing the harmonic composition of the consumed current and by the high value of $\cos\varphi$;
- minimum rated power for elements of the charge device.

The analysis of the used methods for charging the capacitors has shown that, as a rule, they cannot meet to the full extent all the listed above requirements.

It is known that the maximum efficiency of a charge circuit is provided by charging a capacitance with a constant value of current [39]:

$$\eta = \frac{1}{1 + 2k^2 \cdot \frac{RC}{T}},$$

where $k = I_{ef}/I_{av}$ is the charge current form coefficient (I_{ef} is the effective current value, I_{av} is the average current), R is the active resistance in the charge circuit, C is the capacitance, T is the charge time.

In this context, the optimal system is the one providing the charge of the capacitance from a voltage source with a constant current ($k = 1$). The charge of capacitance with a constant current, widely used in the world, is performed by means of a phase control over the mains pulses or by means of a pulse–duration modulation of the source. But the conclusion that the converter efficiency is maximal under a condition of a constant charge current is true only if the converter contains a single circuit. Electrical circuits of converters (from voltage sources to current sources) contain no less than two current circuits. When the charge current in the converter output circuit is constant, but the constant current from an input circuit source cannot be provided, the condition of minimum relative energy loss cannot be met.

A general calculation of the charge device efficiency is given in [39]. Main conclusions of this study are presented below.

According to [39], a circuit of the charge device with an ideal converter without loss is given in Fig. 35. The input circuit losses are accounted by a resistance R_1 and output circuit losses

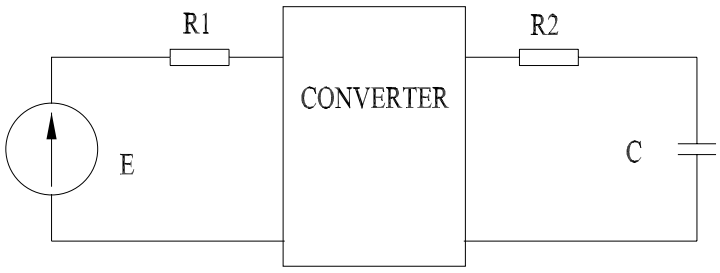

Figure 35: Circuit of charge device with ideal converter without loss.

are accounted by a resistance R_2. The efficiency of the charge device η obviously equals to:

$$\eta = \eta_1 \eta_2,$$

where η_1 is the input circuit efficiency, and η_2 is the output circuit efficiency. As a result the authors obtain the following equation:

$$\eta = \frac{0.5 + \sqrt{0.25 - k_1^2 \frac{P}{P_k}(1 + 2k_2^2 \frac{R_2 C}{T})}}{(1 + 2k_2^2 \frac{R_2 C}{T})},$$

where k_1 and k_2 are coefficients of the current forms at the converter input and output (charge) circuits, P is the mean charge power on the capacitance C, P_k is the short-circuit power of the collider feeding system. (The effect of P_k on the choice of type of the charge device will be observed further).

Imagine the charge device, where the capacitance periodic charge is produced from a constant voltage source via an ideal voltage-current converter. The converter contains a device providing relative duration of charge current pulses, or a device for the phase control of mains pulses, and is used for keeping the time independent charge current. It is obvious that then the capacitance voltage and instantaneous power after the conversion will be linearly increased in time. As our converter does not contain a energy storage, comparable with the energy of the modulator capacitor, the instantaneous power at the converter input repeats the instantaneous power form after the converter. The conclusion is the following: the charge system with a time-constant current in the capacitor charge circuit, loads the power system from the saw law, when the power consumed (inside the charge interval) starts from zero and ends with a doubled value with respect to the mean charge power.

The input current form factor for this device is $k_1 = 1.16$, the efficiency of the charge device is decreased, but there exists a more important factor, which can make it impossible in principle to connect the device to the power system without special measures taken. This concerns the energy consumers whose mean power makes hundreds of MW.

An over two–fold "attack" on the power system with respect to the mean power caused by the DC charge will lead to a contradiction with the electro-technical standard for the electrical energy quality (Grundsätze für die Beurteilung fon Netzrückwirkungen, Frankfurt am Main, 1992), stipulating the value of tolerable excitations in the mains. For the modulator operation frequency of 5 Hz this value is set by the standard to be around 0.55%.

Using this standard, let us find the short circuit power S_k [44] of the power system, which should be provided in the TESLA connection point in order the collider operation not to impair other power consumers:

$$\delta U = 100 \cdot \frac{\Delta Q}{S_k},$$

δU is the value of electricity network disturbance, that is allowed by the standard for the 5 Hz frequency of the collider operation (in %), ΔQ is the peak of the consumed reactive power.

We determine ΔQ supposing that TESLA will have 604 modulators, each consuming 100 kW of average power P_c:

$$\Delta Q = 2P_c \cdot 604 = 1.208 \cdot 10^8 \text{ VA}.$$

And then we determine S_k as:

$$S_k = 100 \cdot \frac{\Delta Q}{\delta U} \simeq 2.2 \cdot 10^{10} \text{ VA}.$$

Charging of TESLA modulator capacitances by DC current, which is good from the point of efficiency, requires to arrange a 22 GVA power of the mains short circuit at the collider connection point S_k.

A well known and widely used circuit in the world is a diode–resonant circuit of the capacitance charge. Such a charge is based on charging the capacitance to a double voltage value of the power supply by a current half–sinusoid which occurs during the power supply commutation to the capacitance under charge through a choke. Though the device operates with good reliability it has some drawbacks. The charge choke should be designed for one forth of the transmitted energy, and the step–up transformer should have a high rated power and large dimensions. But the main disadvantage of this circuit consists in the periods in the charge cycle when the power consumption is zero or equal to 1.57 of the mean consumed power. The diode–resonant charge makes it impossible to vary the repetition rate of the modulator without impairing the quality of the electrical energy. Besides, in this case there may also occur some violation of the standard with respect to the non–sinusoidal coefficient, which following the Russian standard should not

exceed 5%. It should be also noted, that in our case the diode–resonant circuit is scarcely applicable, since the capacitor discharges during one cycle of the modulator operation down to 0.85 of the maximum voltage.

For its powering there should be needed an adjustable rectifier with a voltage close to the maximum capacitance voltage. In this case the capacitance must be reliably protected against a two–fold voltage (compared to the operation value) in case of an emergency drop of the capacitance voltage to zero. Let us estimate, as for the case of a DC current charge, the value of S_k at a diode-resonant charge. It is known that for such a system the power consumption equals zero inside the charge interval (the beginning and the end of the charge half-sinusoid), and equals 1.57 of the mean consumed power (the middle of the half-sinusoid). Then, as above, we have:

$$\Delta Q = 1.57 P_{av} n = 9.5 \cdot 10^7 \text{ VA}.$$

For this case the short circuit power of the power system S_k is:

$$S_k = 100 \cdot \frac{\Delta Q}{\delta U} \simeq 1.73 \cdot 10^{10} \text{ VA}.$$

The above reasoning concerning the DC current charge and the diode-resonant charge of the capacitance are for the mode, when during the modulator operation the capacitance is charged and discharged from zero voltage to its nominal voltage value. The situation with kicks in mains is improved in the case when the capacitance is partially discharged in the modulator operation cycle, as it is done at the Fermi Laboratory for the TESLA modulators. Here the capacitance current does not reach the zero value inside the charge interval. Decreasing the mains kick value, this system, nevertheless, does not solve the problem. In the charge current waveform of the modulator capacitance, that is presented by Fermilab, the maximum current value is 1.424 times greater than the minimum one. Let us find the short circuit power of the power system S_k, and for this case:

$$S_k = 100 \cdot \frac{\Delta Q}{\delta U} \simeq 4.656 \cdot 10^9 \text{ VA}.$$

The obtained value of the short circuit power exceeds the TESLA mean consumed power by about two orders of magnitude. There is one more significant disadvantage of this charge system, related to the fact that the system is based on a phase controlled thyristor rectifier, but we shall consider it below.

The value of the charge device efficiency and its optimal interaction with the power system is basically determined by a feasibility to transfer the energy to the converter at a constant power [40]. Such a system does not have the above shortcomings and has the following advantages:

- a higher source utilization factor – this allows to decrease its mass;
- minimum possible losses in the converter input/output circuits;
- low-frequency "shocks" upon the power system (with collider repetition rate), hampering the operation of other consumers, are eliminated;
- meets criteria for charge devices, listed at the beginning of this chapter.

7.2 The choice of scheme of the power charge device

BINP has successfully tested a charge system consuming a constant power of 300 kW from the mains, which consists of three 100 kW modules. The basic part of the module is a thyristor inverter converting the input voltage into current pulses at a high repetition rate, charging in portions the capacitor up to the required voltage through the step–up transformer. The module operation is described in more detail in [41]. Below in this paper will be also described the module operation in its application to our task. A sketch diagram of the device is given in Fig. 36.

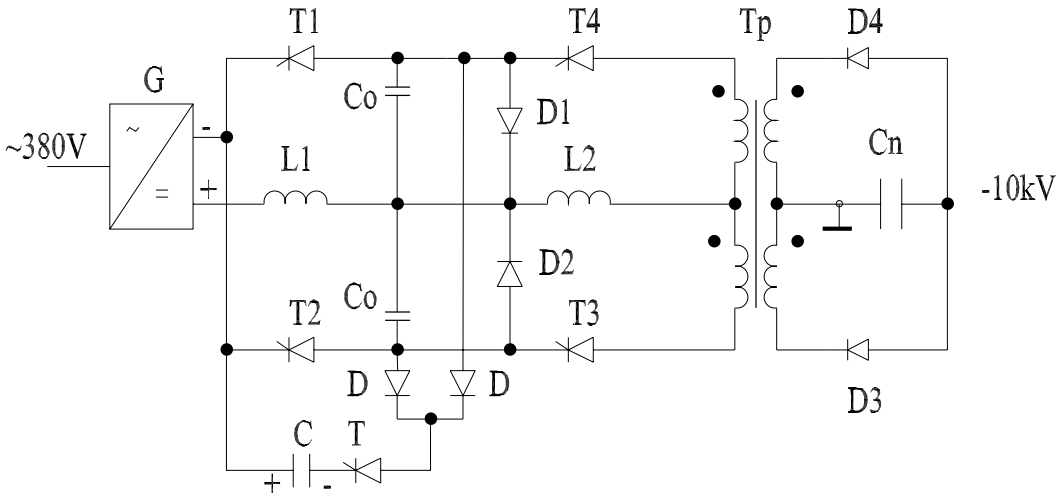

Figure 36: Simplified circuit diagram of a charge device with an electron protection.

The inverter consists of two loops. The first loop consist of a mains rectifier G, thyristors T_1 and T_2, a choke L_1 and dosing capacitors C_0, the second loop includes a capacitors C_0, thyristors T_3 and T_4, diodes $D_1 \div D_4$ and a storage capacitor C_n. The step-up transformer T_p used only to transform the inverter output voltage. Its design is shown in Fig. 37. The inverter works in

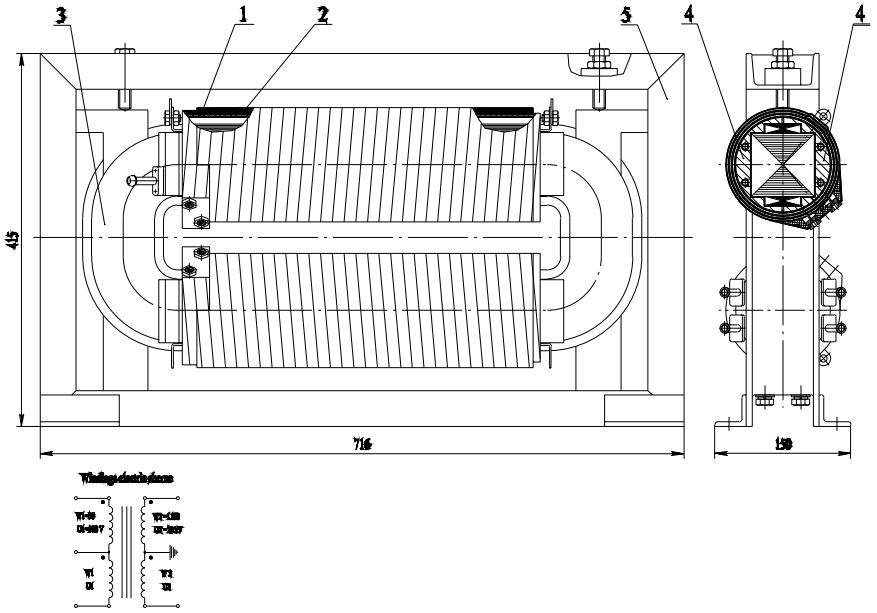

Figure 37: Charge transformer. 1 – primary winding, 2 – secondary winding, 3 – core, 4 – water–cooling insert, 5 – framework.

the following way. Capacitors C_0 are charged in succession from a low–voltage mains rectifier G up to its two-fold voltage by switching on thyristors T_1 and T_2 through the inductance L_1. Every half–period of the inverter operation they transfer their energy to the capacitor C_n, being discharged by switching thyristors T_3 and T_4 through the inductance L_2 to the primary winding of the transformer T_p. For a complete energy transfer from C_0 to C_n they are shunted by diodes D_1 and D_2. With the help of these diodes there is no over-charging of the capacitors C_0, the energy is completely transfered to capacitor C_n and there are provided initial conditions for the next charge cycle. The last process is the most principle one in the inverter operation. We have

the situation, when the rectifier inside the charge interval works to dosing capacitors with zero initial conditions: $U_{Co} = 0$.

But the capacitors C_0 are discharged completely with a full energy transfer to the storage capacitor C_n only to the value $U_{Cn} = U_G \cdot n$ ($U_G = 500$ V is the voltage at the rectifier, n is the transformation ratio of the transformer T_p). With a further increase in the voltage on C_n, the capacitors C_0 do not discharge completely, which leads to a reduction in the average value of the consumed current and a violation of the constant power consumption from the mains. The capacitor charging is finished at $U_{Cn} \simeq (1.05 \div 1.1)U_G \cdot n$, which is the maximum tolerable over-voltage in the circuit. Thus, the range $0 < U_{Cn} \leq U_G \cdot n$ is the condition for the optimal operation at a constant power consumption.

The control of the charge voltage level is performed by varying the pulse repetition rate of the inverter. The maximum repetition rate corresponds to the continuous inverter operation and the maximum charge voltage. The voltage decreases with the pulse repetition rate. The thyristors T_1, T_3 and T_2, T_4 are triggered by means of a functional "voltage-frequency" converter which is controlled with the help of a variable reference voltage. In case it is necessary to compensate parametric instabilities of the modulator elements, it is possible to compare the signals from the gauges with the reference voltage.

As is known from [40], the operation of a single charging device, provided the mean power consumed from the mains is constant, is characterized by ripples with drops to zero in the intervals between the charge pulses. At a maximum inverter repetition rate the phase shift between the sinusoidal charge pulse of the current is equal to π. In this case, the efficiency coefficient $k_{ef} = I_{av}/I_{max}$ (I_{max} - maximum value of current) is equal to 0.637 and decreases with the increase in the phase shift during the voltage drop in the process of control. The multi phase design of the charge system decreases fluctuations (rippling) and makes the efficiency coefficient equal to $k_{ef} = 0.9$ in the two–phase variant for the phase shift by $\pi/2$, 0.95 and 0.97 in the three – and four – phase variants, respectively. In our case, when it is planned to use 604 modulators for the TESLA collider, the problem of the mains loading with a constant power is automatically solved. To which extent the power consumption from the mains is constant can be estimated from the formula [40]:

$$k_{ef} = \frac{2m}{\pi} \cos(\frac{m-1}{2m}\pi) = 0.9999988,$$

where $m = 604$ is the number of modulators.

Hence, TESLA, if it has the proposed capacitor charge device, can operate consuming a constant power from the mains in a wide interval of voltage adjustment, or variation in pulse repetition rate of the modulator operation cycles. Such a mode of the accelerator operation is probably needed for adjustment, preventive maintenance and other work, when the maximum intensity of the accelerated current is not required.

The problem of smoothly switching on the load into the mains (as well as its switching off) and of a slow growth (drop) of the consumed power is solved by applying the reference voltage to the functional "voltage – frequency" converter through a timer circuit.

The inverter does not require an insulating mains transformer in the rectifier G. Either one, or a number ($10 \div 20$) of inverters can operate from one high-current rectifier. Between the rectifier and the inverter an electron switch is used. It works together with emergency switches which are of a comparatively slow action. The protection circuit (see Fig. 36) operates as follows: the capacitor C, charged from the low power rectifier ($50 \div 100$ W) in the indicated polarity, is in a waiting mode. During the alarm situation, for example, when the operation fails or the inverter sticks, the rectifier current feeding the inverter goes out of the design mode. In this moment, when it reaches the determined level, the thyristor T is switched on by a comparator signal, and the reverse voltage from the capacitor C is applied to the inverter thyristors T_1 and T_2, at the same time the trigger pulses are taken off. The thyristor which was switched on at that moment (T_1 or T_2), switches off, the inverter alarm current is taken over by the circuit:

the capacitor C, thyristor T, and one of diodes D. After the polarity reversal of the capacitor C, the thyristor T is switched off, and the protection circuit is restored.

It seems advantageous to employ the following scheme of a power supply for the TESLA modulators:

- a rectifier ($\sim$ 380 V/=500 V) for powering several HVS (10 – 20 pieces) for a mean power of $1 \div 2$ MW and more is located in the energy center;
- each inverter is located near the modulator. It is connected to the rectifier through a contactor;
- the contactor is remote–controlled; in emergency situations it is automatically disconnected.

Such a configuration is economically justified, because the location of the inverter in the energy center requires the use of an expensive high voltage cable from the inverter to modulator. A DC feedline will be considerably cheaper, and DC electrical losses will be considerably lower.

Note one more feature of the proposed charge device – it is powered from a non-controlled diode rectifier. As discussed above, many of charge devices (the charge system from Fermilab is among them) are based on thyristor rectifiers, where the capacitor charge mode is preset by a thyristor switch phase. As a rule, the thyristor switch phase is close to π at the beginning of the charge interval, and as the capacitor is being charged, it decreases, approaching at best the value of the mains phase, i.e. $\pi/3$. This fact impairs the harmonic composition of the consumed current and leads to a change of $\cos\varphi$ (shift of voltage and current vectors) inside the charge interval. The conclusion is that for a charging device based on rectifiers with thyristor regulators:

a) there is no compensating odd harmonics, because the relationship between their amplitudes constantly varies;

b) there is no completely compensating $\cos\varphi$.

The charge systems with thyristor regulators reduces the rectifier power factor. It is known [42] that the rectifier power factor χ depends on the shift factor $\cos\varphi$ as well as on the distortion factor ν:

$$\chi = \nu \cdot \cos\varphi.$$

Both the factors ν and $\cos\varphi$ are notably reduced when coming to a deep regulation – this is a significant disadvantage of the charge systems based at the rectifiers regulated with a help of a line voltage angle α.

A constant power charge device for capacitors operate from a non-controlled diode rectifier. As this rectifier is loaded by a big number of LC circuits, the initial conditions of which are constant, and the rectifier current is fixed, the diode commutation angles will be mainly determined by parasitic parameters of the step – down transformer and electrical circuits before it. In such a system $\cos\varphi$ will be constant and negligibly small, and the physical picture will be as if we switched on a three – phase rectifier to an active resistor.

Note some disadvantages of the charge system described:

- the charge device is based on the inverter, that is, as a powerful frequency converter, a source of radio interference voltage. That is why it is necessary to connect an interference filter at its input. The industry produces a great number of interference filters for different currents and voltages with a working damping of 60, 80 and 100 dB;
- the inverter is a source of noises of the sound range; the main sources of noise are the chokes L_1 and L_2, and transformer T_p (see Fig. 36). We partially decrease this disadvantage placing these elements in a tank filled with transformer oil.

In conclusion note, that it is no good using serial inverters produced by different manufacturers for industrial purposes in the charging device. This inverters cannot provide the constant power consumption mode, as these are one-circuit systems (they are based on a IGBT transistor or thyristor bridge). The device suggested here has two circuits, and the circuit connected to the mains operates so, that while transmitting the energy to the modulator capacitance, the dosing capacitors C_0 discharge to zero inside the charge interval at each cycle of the inverter operation, and their initial conditions are not changed.

7.3 Choice of the inverter operation frequency

The operation frequency of the inverter was chosen taking into account most uncostly electronics and electro-technical components, the optimization of the inverter elements by the mass – size parameters, and the method of the voltage stabilization on the capacitance.

The maximum frequency of the inverter operation is determined by the characteristics of the thyristors used, in particular by the time of their switch off. The analysis made at BINP shows that at acceptable energy parameters of the choke L_2, to be optimized by its mass minimum and the efficient value of the current transmitted to the capacitance, the switch off time t_{off} may make $10 \div 15\%$ of the duration of the charge current half – sinusoid. The industry produces comparatively cheap inverter thyristors with a switch off time of $10 \div 15$ μs. Thus, the availability of parts makes it possible to choose the duration of the inverter frequency half – period up to 100 μs. The upper limit for the frequency may be defined by the choice of the ferromagnetic for electro-technical components of the inverter. The main factor will be the idea to use inexpensive electrical cold – rolled steel. These steels up to frequencies of 3 kHz are beyond competition compared to Permalloy.

Overall dimensions and the required stability of the charge voltage on the capacitance set a limit on the inverter operation frequency from below. Taking into account that the charge current of the capacitance has a form of a half – sinusoid and the operation of the inverter is not synchronized with that of the modulator, it becomes evident that the modulator can act when the charge current is at the half – sinusoid peak or zero. Let us estimate the stability of the capacitance voltage with an accuracy of up to one charge pulse. The below formula serves for calculating the stability:

$$\frac{\Delta U}{U} = \frac{1}{2n} \cdot (1 - k^2),$$

where n is a number of the charge pulses during the charge period, $k = \frac{U_1}{U_{max}}$ is the relation of the capacitance voltage after the working cycle of the modulator to its maximum value.

Considering the above, there was chosen an inverter with an operation frequency $f = 500$ Hz. Let us calculate the voltage stability on the capacitance, keeping in mind that the number of charge pulses $n = 200$ per one operation cycle. Our estimation is for two cases:

- B-modulator or modulator based on mismatched PFN

$$\frac{\Delta U}{U} \simeq \pm 7 \cdot 10^{-4};$$

- modulator based on matched PFN with $k = 0$

$$\frac{\Delta U}{U} \simeq \pm 2.5 \cdot 10^{-3}.$$

If this frequency is used, it becomes unnecessary to introduce a system of dividing one charge pulse in the charge inverter, which simplifies the device and its control algorithm, increases its reliability and reduces the cost. And finally note, that the chosen frequency is near the industrial one of 500 Hz, so following the detailed investigation of the problem, it seems quite probable to find a firm producing suitable electro-technical components.

8 Conclusion

Following the calculations presented in the above chapters, the following values of efficiency of the main elements (parts) of the modulator have been obtained, in case of an optimal choice of the modulator and the feedline, 1.7 km long:

- PFN with a feedline and a pulse transformer – $\eta_M = 0.9$;
- Charge device – $\eta_{CD} = 0.95$

The total efficiency of the modulator based on a mismatched PFN will make:

$$\eta = \eta_M \cdot \eta_{CD} = 0.855.$$

On the basis on the work performed on the paper study of the modulator for the power supply of a 10 MW TESLA klystron, the following conclusions can be drawn:

- there was done an analysis of the klystron breakdown mechanism and there were suggested methods of estimation of the energy release in case of a breakdown;
- there was proposed and developed a design of the pulse transformer with low parasitic parameters and an effective protection against overloads at probable klystron breakdowns;
- there was proposed and studied a circuit of the device forming the voltage pulse based on a mismatched PFN, which simplifies the design of the modulator and makes the modulator cheaper, reduces the energy intensity of the storage capacitor, simplifies the klystron protection at a breakdown of a high voltage switch, and replaces harmful mercury ignitrons with thyristors (diodes);
- there were analyzed and proposed variants of design for low voltage and high voltage feedlines, analyzed the influence of the feedline on the pulse distortion and losses in the modulator, the choice was made at the present stage in favor of low voltage feedline;
- there was proposed a high-efficiency charging device, providing for a constant power takeoff from the mains with minimum fluctuations and distortions.

It should be noted that in order to build a modulator, which would make a prototype for the further multiple production, one should carry out a big job on detailed calculations, design and development of all parts and units of the modulator, as well as on on the simulation and modeling of the modulator.

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Budker INP 2002-59

Ответственный за выпуск А.М. Кудрявцев
Работа поступила 21.10.2002 г.

Сдано в набор 23.10.2002 г.
Подписано в печать 24.10.2002 г.
Формат бумаги 60×90 1/16 Объем 3.7 печ.л., 3.0 уч.-изд.л.
Тираж 110 экз. Бесплатно. Заказ № 59

Обработано на IBM PC и отпечатано на
ротапринте ИЯФ им. Г.И. Будкера СО РАН
Новосибирск, 630090, пр. академика Лаврентьева, 11.