ИНСТИТУТ ЯДЕРНОЙ ФИЗИКИ
им. Г.И. Будкера СО РАН

V.M. Aulchenko, A.E. Bondar, V.P. Nagaslaev,
A.A. Tatarinov, V.M. Titov

THE STUDY OF NONSTANDARD MODES OF CAMEX OPERATION WITH SHORT BUNCH CROSSING TIME

BUDKERINP 94-9

НОВОСИБИРСК

The study of nonstandard modes of CAMEX operation with short bunch crossing time

V.M. Aulchenko, A.E. Bondar, V.P. Nagaslaev, A.A. Tatarinov, V.M. Titov

Budker Institute of Nuclear Physics,
630090, Novosibirsk, Russia

Abstract

The study of the possibility to use CAMEX chip in several systems of the detector KEDR at the e^+e^- collider VEPP-4M was performed. The relatively short bunch crossing time at VEPP-4M 600ns leads to some problems with the use of CAMEX in the standard mode. The different ways to overcome these difficulties are investigated and compared.

Introduction

A new multipurpose experiment KEDR [1] for high energy physics at the storage ring VEPP-4M is being constructed now. Two systems of the detector: the photon spectrometer at zero angles and the microvertex detector are planning to exploit microstrip chambers. That makes one to search for the choice of the highly integrated multiplexing readout electronics. One of the possible implementations is CAMEX. However, the use of CAMEX has its own peculiarities, as it had been developed specifically for LEP experiments, where the bunch crossing time is about 20 mks, while being 600 ns at VEPP-4M. In a work [2], performed in our institute earlier, there was shown that the speed features of CAMEX make it fast enough. There was also suggested a new mode of operation to realize all advantages of chip within the 600 ns accelerator cycles.

Several characteristics of CAMEX in this regime are studied in this paper.

CAMEX and regimes of its operations

The CAMEX chip is a crystal of 6.4×5 mm^2 size. It contains 64 channels and a decoder for the sequential readout. There is a charge-sensitive amplifier with a circuit of multiple correlated sampling (Fig. 1). The controlled switches R1 and R2 clear the capacities Cf1 and Cf2 correspondingly, the switches S1–S4 connect the storage capacities to the CSA1 output.

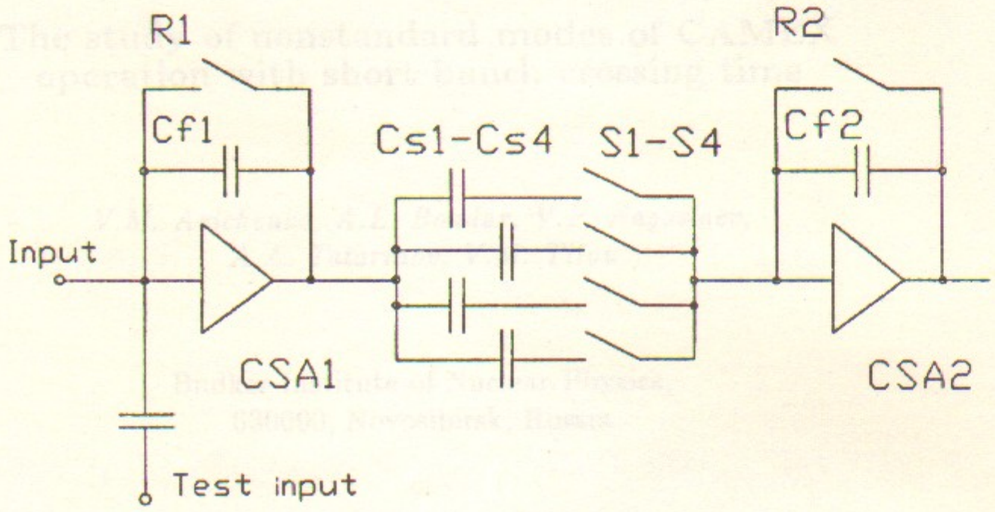

Fig. 1. The layout of one Camex channel.

Let's describe several possible regimes of CAMEX operation. In a standard regimes (Fig. 2) some preparatory operations are done before the signal can arrive. The capacity Cf1 is cleared and preliminary samples done and stored in Cs capacities. The switch R2 this time is closed. Then the device is ready to receive a signal from the detector.

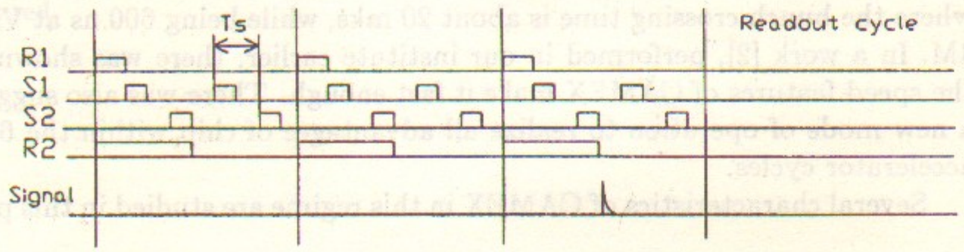

Fig. 2. Standard Camex cycle.

After the signal has come samples are taken again for each of the capacities Cs while the switch R2 is open. The charge flown to Cf2 in each of the samples is equal to the difference of the charge came to the Cf1 after the signal appeared (signal+noise) and before (noise only). One thus obtains an improved signal/noise ratio (as a square root of the sample number). In this regime the cycle period has to be equal to the bunch crossing time, i.e. 600 ns. However, the measurements [2] have shown that when the time Ts

(Fig. 2) is less than 160 ns (note, time of switches S1–S4 being on is half of Ts), the gain drops significantly due to the insufficient rapidity of the chip. That's why only 2 samples of noise and 2 sample of signals are accessible during the cycle.

To improve the rapidity one can make use of the asynchronous regime (Fig. 3). The first tact in regime is preparatory. 4 samples are taken and then the device waits for the signal coming during some time Texp. If the signal has not come the cycle is generated again. If the signal appeared, Cf2 is cleared and 4 samples are taken, then the reading cycle is started. In real circumstances, however, there exist leakage currents, beam and RF pick-ups, background particles and SR photons hits in a detector. All these sources may cause the piling of the charge in Cf1 and Cs capacities during long time Texp, restriction of the amplifier dynamic range, pedestal level shifts, noise growth, etc. All these parameters have to be carefully measured in respect to the expectation time to find the optimal Texp.

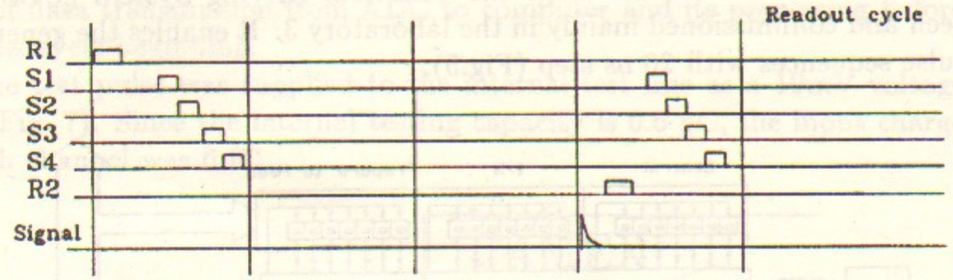

Fig. 3. Asynchronous cycle.

Another way to improve the rapidity is to use the nonstandard cycle which is the combination of the described above ones, (Fig. 4).

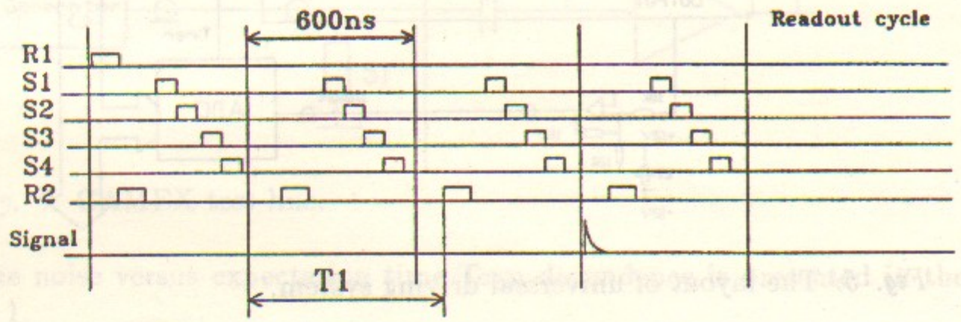

Fig. 4. "Nonstandard" cycle.

In the first tact Cf1 and Cf2 are cleared and 4 preliminary samples are taken. The latter tacts differ from the former only by that Cf1 capacity is not cleared there. Like in asynchronous regime, the cycle one continues over some time Texp, and then restarts again. If during the time Texp the signal occurs (say, in n-th tact), the cycle stops and reading cycle starts. Thus the samples taken in $(n-1)$-th tact are subtracted from the samples taken in n-th tact, and the output pulse is proportional to the charge came during the last tact.

The same problems those in asynchronous mode may arise, so the measurements of the dynamic range and pedestal levels for a combined one are represented as well.

Results of the measurements
Asynchronous regime

To drive the CAMEX chips the Universal Driving System (UDS) had been and commissioned mainly in the laboratory 3. It enables the generating pulse sequences with 20 ns step (Fig.5).

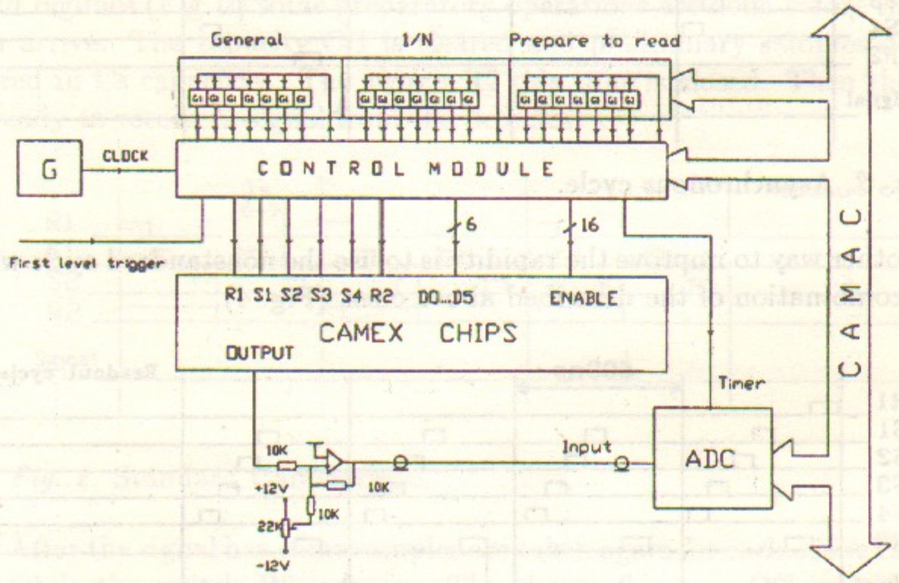

Fig. 5. The layout of universsal driving system.

In order to measure the parameters of asynchronous regime the time diagram shown in Fig. 6 had been realized. All the switches were closed until the cycle start. The sample time Ts was 80 ns and there were no intervals

between the driving pulses S1–S4. In the first tact preparatory samples S1–S4 were taken, then in a proper moment the test pulse was introduced, the capacity Cf2 were cleared and the reading cycle started.

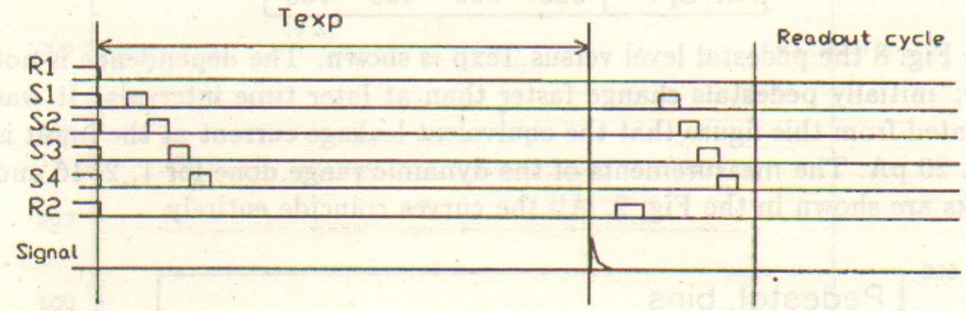

Fig. 6. Asynchronous cycle as used in this work.

After reading all 64 channels all the switches were closed again for the time of data transmission from ADC to computer and its processing before the new cycle beginning.

The test pulse was supplied to the internal test line as a 10mV voltage step (Fig. 7). Since the internal testing capacity is 0.6 pC, the input charge in each channel was 6 fC.

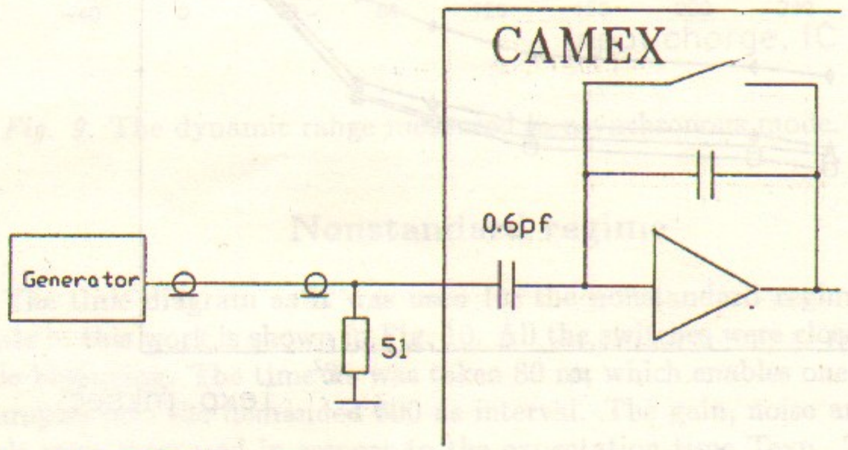

Fig. 7. CAMEX test line.

The noise versus expectation time Texp dependence is presented in the Table 1.

Table 1.

Texp, us	1	2	80	500
ENC, e^-	520	520	590	700

In Fig. 8 the pedestal level versus Texp is shown. The dependence is not linear: initially pedestals change faster than at later time intervals. It was estimated from this figure that the equivalent leakage current at the input is about 20 pA. The measurements of the dynamic range done for 1, 2, 16 and 40 mks are shown in the Fig. 9. All the curves coincide entirely.

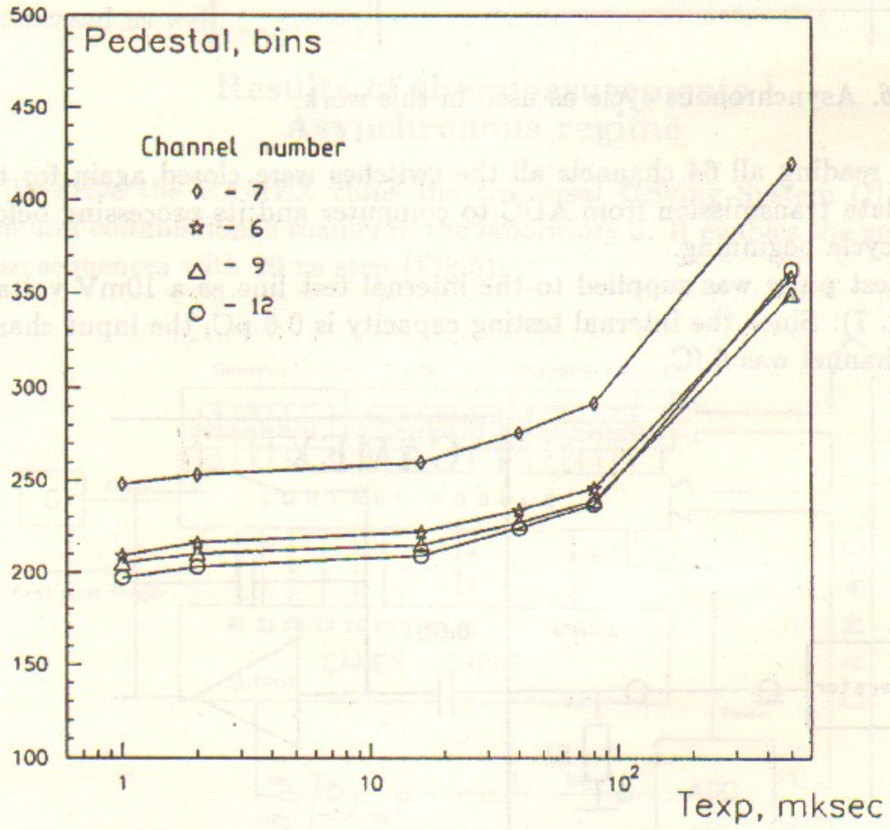

Fig. 8. The dependence of pedestal levels on the signal expectation time.

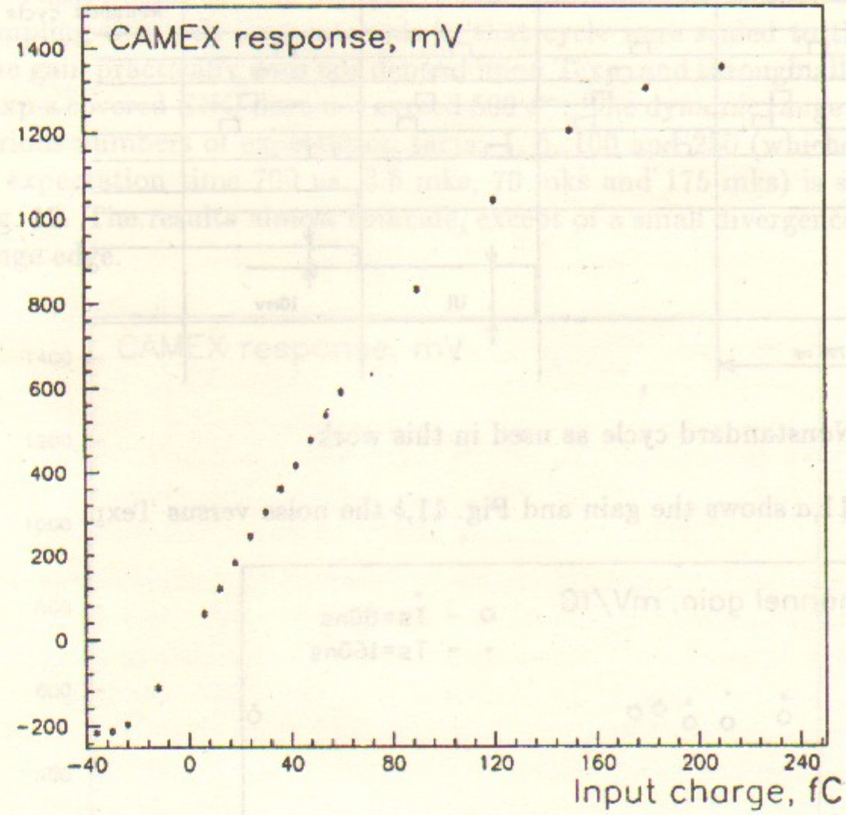

Fig. 9. The dynamic rahge measured in asynchronous mode.

Nonstandard regime

The time diagram as it was used for the nonstandard regime measurements in this work is shown in Fig. 10. All the switches were closed until the cycle beginning. The time Ts was taken 80 ns, which enables one to pack all 4 samples into the demanded 600 ns interval. The gain, noise and pedestal levels were measured in respect to the expectation time Texp. To measure the gain and the dynamic range the step voltage step pulse had been supplied (U_{in1}, Fig. 10).

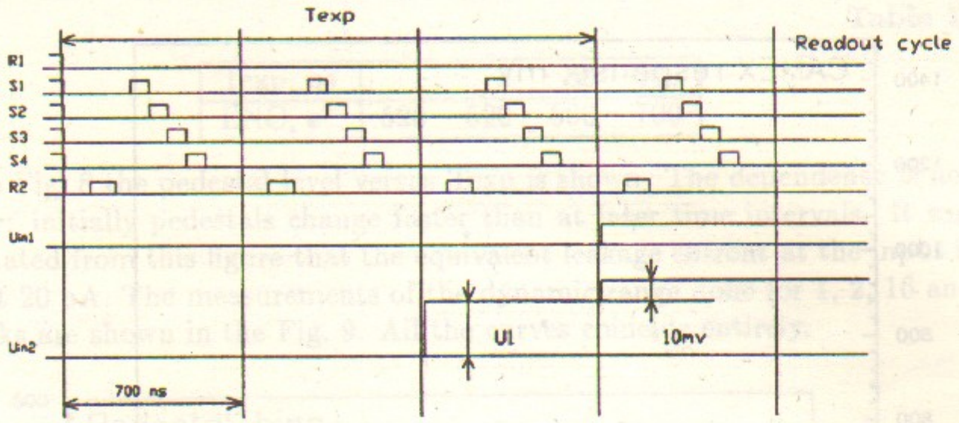

Fig. 10. Nonstandard cycle as used in this work.

The Fig. 11,*a* shows the gain and Fig. 11,*b* the noise versus Texp.

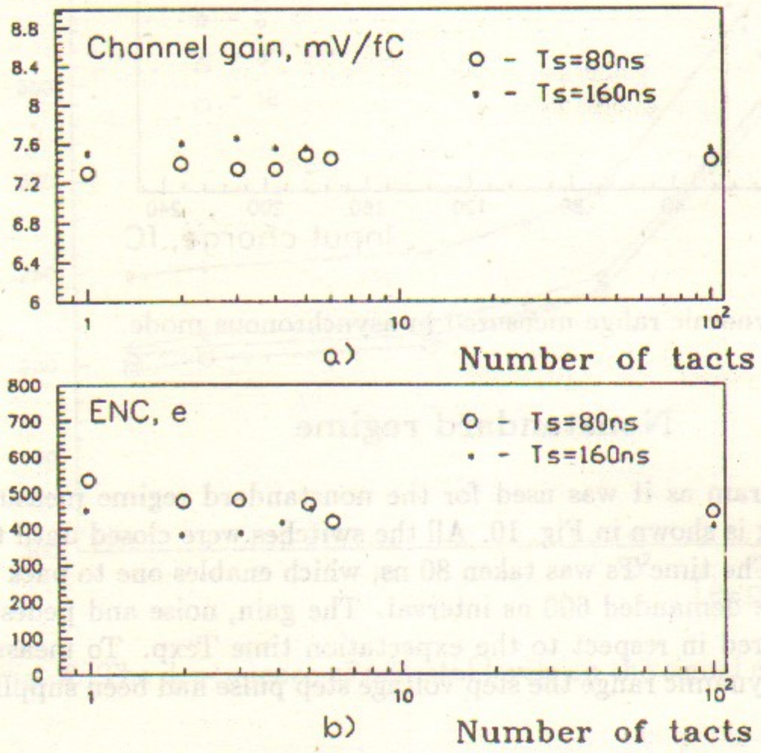

Fig. 11. The gain (a) and ENC (b) dependence on the number of tacts in a combined mode. The time of one tact is 700 ns for Ts=80 ns and 1400 ns when Ts=160 ns.

These figures contain also the results of measurements made with 160 nsec sampling time (all time intervals in that cycle were scaled to the factor 2). The gain practically does not depend upon Texp, and through all the range of Texp-s covered ENC does not exceed 500 e^-. The dynamic range obtained for various numbers of expectation tacts: 1, 5, 100 and 250 (which corresponds to expectation time 700 ns, 3.5 mks, 70 mks and 175 mks) is shown in the Fig. 12. The results almost coincide, except of a small divergence seen at the range edge.

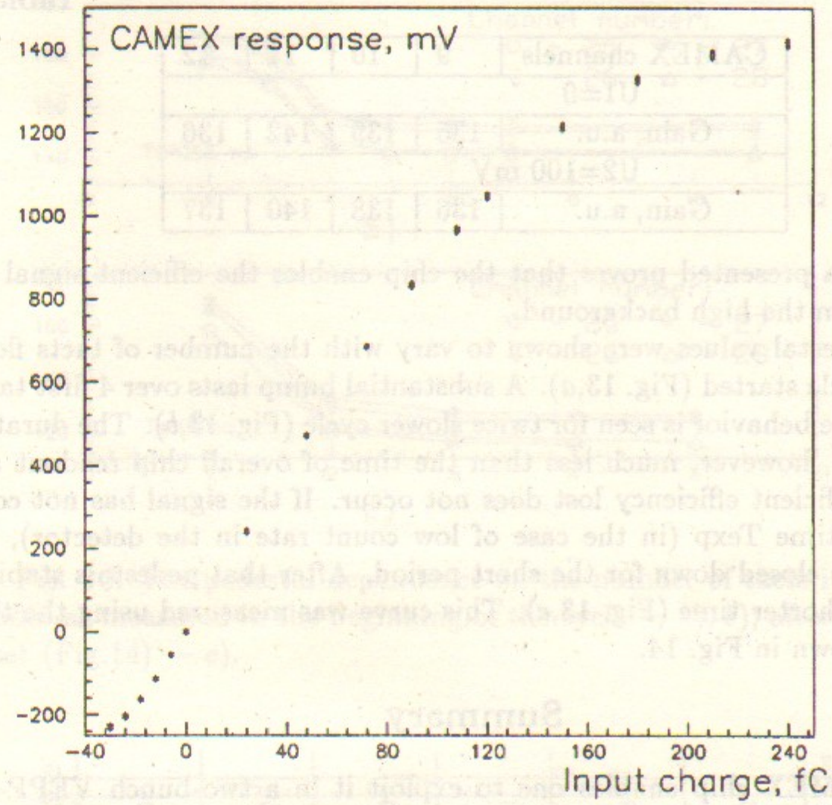

Fig. 12. The dynamic range measured in a combined mode.

Then, the efficiency of the background charge subtraction was checked, which may leak from the detector during considerable time Texp. To model such a situation the two steps pulse shape has been made (U_{in2}, as shown in Fig. 10). The first step simulates the background, it's value varying between 0 and 200 mV. The second step was a signal to be measured and it's value was 10 mV. The step voltage 100 mV corresponds to the 375000 e^- charge at the input. The dependence of pedestals (first step only) and the gain on

the U1 voltage were measured and presented in Tables 2 and 3.

Table 2.

U1, mV	CAMEX channels			
	9	10	11	12
0	130	116	120	114
100	128	115	118	112
200	129	117	118	113

Table 3.

CAMEX channels	9	10	11	12
U1=0				
Gain, a.u.	135	139	142	136
U2=100 mV				
Gain, a.u.	136	138	140	137

The data presented proves that the chip enables the efficient signal extraction from the high background.

The pedestal values were shown to vary with the number of tacts flown after the cycle started (Fig. 13,*a*). A substantial bump lasts over 4 first tacts.

The same behavior is seen for twice slower cycle (Fig. 13,*b*). The duration of 4 tacts is, however, much less than the time of overall chip readout and thus the sufficient efficiency lost does not occur. If the signal has not come during the time Texp (in the case of low count rate in the detector), the switch R1 is closed down for the short period. After that pedestals stabilize within the shorter time (Fig. 13,*c*). This curve was measured using the time diagram shown in Fig. 14.

Summary

The CAMEX chip enables one to exploit it in a two-bunch VEPP-4M operation mode, when the time between consequent collisions is 600 ns.

The best chip parameters were obtained when the "nonstandard" mode of operation was realized which is the combination of standard and asynchronous regimes. That makes possible to use all 4 samples unlike in the standard mode. In a difference with asynchronous mode, the background charge, accumulated due to the background particles or the detector leakage does not contribute to the useful signal, thus no pedestal shift neither the noise growth occur during the expectation time.

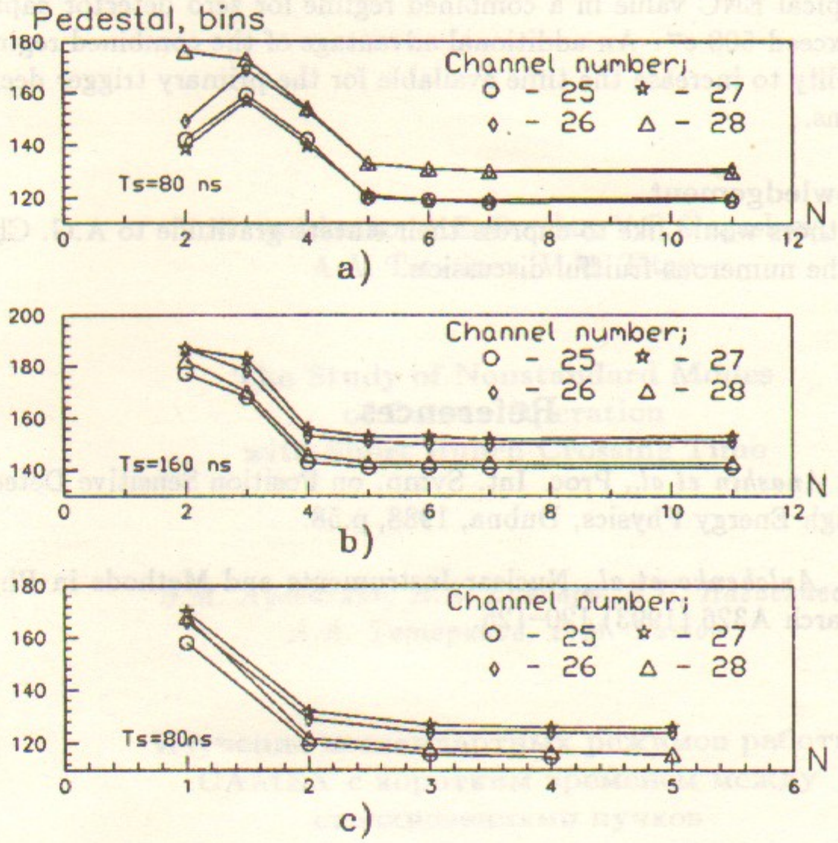

Fig. 13. The pedestal dependence on the number of tacts in a combined mode: as measured in the beginning of the cycle — *a*), *b*); after the short R1 reset (Fig.14) — *c*).

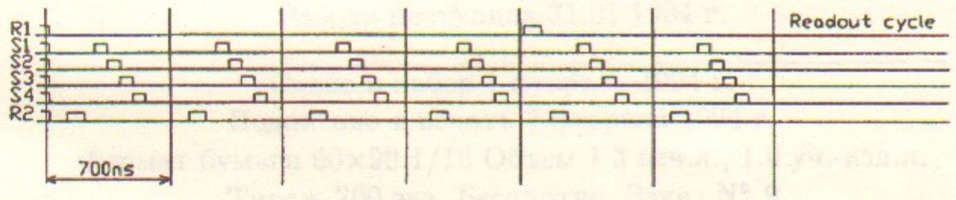

Fig. 14. Short R1 reset after expectation time expired in the combined mode.

The typical ENC value in a combined regime for zero detector capacity does not exceed 500 e^-. An additional advantage of the combined regime is the possibility to increase the time available for the primary trigger decision up to 700 ns.

Acknowledgement

The authors would like to express their sincere gratitude to A.G. Chilingarov for the numerous fruitful discussion.

References

1. *V.V. Anashin et al.*, Proc. Int. Symp. on Position Sensitive Detectors in High Energy Physics, Dubna, 1988, p.58.

2. *V.M. Aulchenko et al.*, Nuclear Instruments and Methods in Physics Research A326 (1993) 120–125.

V.M. Aulchenko, A.E. Bondar, V.P. Nagaslaev,
A.A. Tatarinov, V.M. Titov

The Study of Nonstandard Modes of Camex Operation with Short Bunch Crossing Time

*В.М. Аульченко, А.Е. Бондарь, В.П. Нагаслаев,
А.А. Татаринов, В.М. Титов*

Изучение нестандартных режимов работы CAMEX с коротким временем между столкновениями пучков

Ответственный за выпуск С.Г. Попов
Работа поступила 31.01 1994 г.

Сдано в набор 1 февраля 1994 г.
Подписано в печать 7 февраля 1994 г.
Формат бумаги 60×90 1/16 Объем 1.3 печ.л., 1.0 уч.-изд.л.
Тираж 200 экз. Бесплатно. Заказ N° 9

Обработано на IBM PC и отпечатано на
ротапринте ИЯФ им. Г.И. Будкера СО РАН,
Новосибирск, 630090, пр. академика Лаврентьева, 11.